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Design of Frequency Meter Unit for Low-Power Integrated Circuits

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Abstract: *The development of a circuit and layout of the frequency meter unit for low-power integrated circuits is represented in this article. Simulation results of the device for 90 nm CMOS technology are considered. An estimation of a range of the measurable frequencies for certain values of counter stages at clock frequencies 0.25, 0.5, 1 GHz was carried out. Besides, dependences of power consumption on the frequency of the clock oscillator at the measurable frequencies from 10 MHz to 50 MHz were obtained.*

Keywords: *digital frequency meter, low-power integrated circuits, CMOS VLSI, circuit simulation*

1. Introduction

With rising of integration level of VLSI circuits, requirements to the power consumption of IC elements are increasing [1]. Consequently there is strong demand for low-power circuits. This is especially important for mobile devices with wireless power supply: RFID applications, micro-robots, implantable diagnostic chips, biomedical applications, wireless detection of environmental parameters, navigation. In particular, capacitive sensors, e.g. accelerometers or gyroscopes, require low-power capacitance-to-digital converters [2]. The unit for the frequency measurement with subsequent conversion of the frequency to binary code is considered in this article. The device was designed for implementation in CMOS technology with 90 nm design rules [3].

2. Operating Principle and Design of the Proposed Digital Frequency Meter

A circuit of the frequency meter for the low-power systems, designed using logic editor and simulator DSCH [4], is shown in Figure 1. There are three dotted areas in the figure: 1 – driver of the write delay from the counter to the register, 2 – *n*-stage counter, 3 – *n*-stage parallel register.

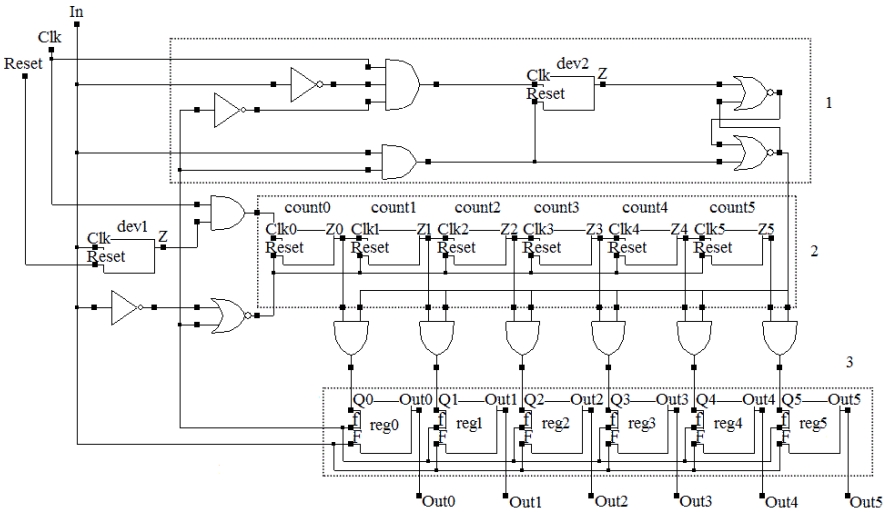

Figure1. *Schematic circuit of the frequency meter unit: 1 – delay driver; 2 – n-stage counter; 3 – n-stage parallel register*

After a short positive pulse has been applied to 'Reset' 'input, during applying the measurable signal with *F* frequency to 'In' input, signal with frequency

$$f = \frac{F}{2} \quad (1)$$

is appearing at output 'Z' of the single-order counter dev1. This enables to measure the signal frequency *F* during its period

$$T_F = \frac{1}{F} \quad (2)$$

At rise edge of the signal *f*, the signal *Clk*, whose frequency is much more than the frequency *f*, flows to 'Clk' input of the *n*-stage counter. Number of clock pulses corresponding to certain binary code arises at outputs of the counter. This binary code is transmitted to parallel register (area 3 in Figure 1) after the delay formed by delay driver (area 1 in Figure 1) and stored during time

$$t = 1.5 \cdot T_F. \quad (3)$$

In this way, the parallel register stores previous state of the *n*-stage counter while the counter performs next measurement. The driver of the write delay from the counter to the register is necessary to prevent concurrence uncertainty, which would appear during transitions of the *n*-stage counter from one state to another. Cell AND3 passes *Clk* signal to the input of *n*-stage counter at the fall edges of signals *F* and *f* and it passes *Reset* signal at the rise edges of these signals. Reset of *n*-stage counter to zero takes place when the rise edge of *F* signal and the fall edge of *f* signal are simultaneously applied. Reset of the parallel register to zero occurs when the rise edges both of *F* signal and *f* signal are simultaneously applied.

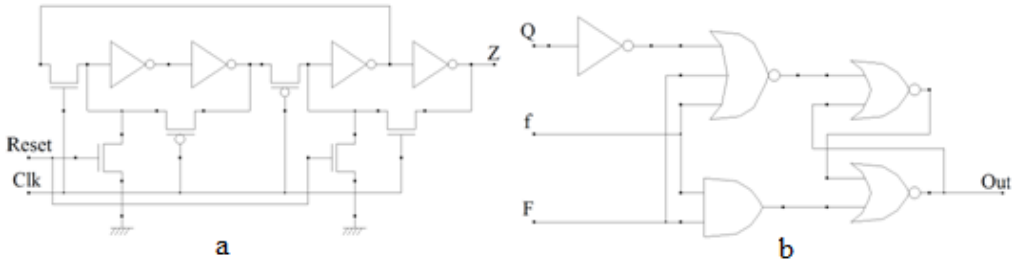

Figure2. *Schematics of the cells: a – schematic of single-order counter [1]; b – schematic of the parallel register cell*

In Figure 2a schematic of single-order counter is shown [1] and schematic of the developed parallel register cell is shown in Figure 2b.

Minimum frequency value, which can be measured by this frequency meter, depends on clock frequency F_{Clk} and the number *n* of the counter stages. Maximum measurable frequency is limited by high-order bit of the *n*-stage counter and it also depends on proper operation of the delay driver.

The layout of the frequency meter unit created using Microwind software tools [4] for 90 nm CMOS technology is shown in Figure 3. The total area occupied by the frequency meter on the chip is about 4077 μm^2.

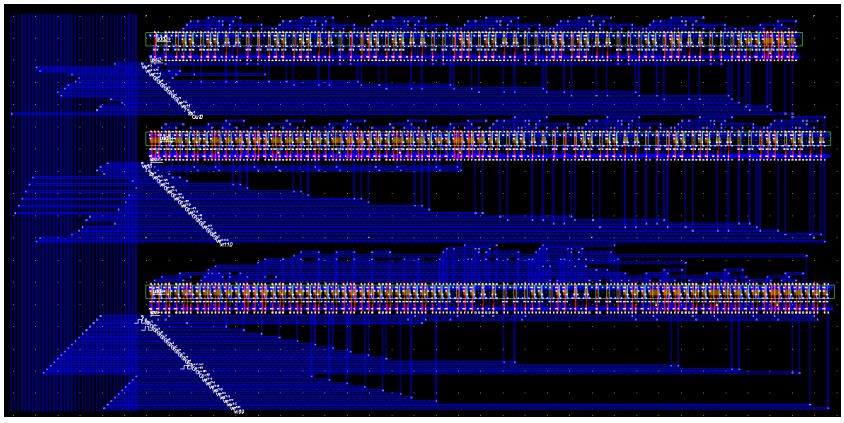

Figure3. *Layout of the frequency meter unit*

3. Simulation And Discussion

The simulation of the frequency meters was conducted using Microwind for number of stages n = 10, clock frequency F_{Clk} = 0.5 GHz and measurable frequency F = 10 MHz. The results of the simulation are shown in Figure 4. The timing diagrams showed in the Figure 4 completely corresponds to the operating principle of the device described in previous section.

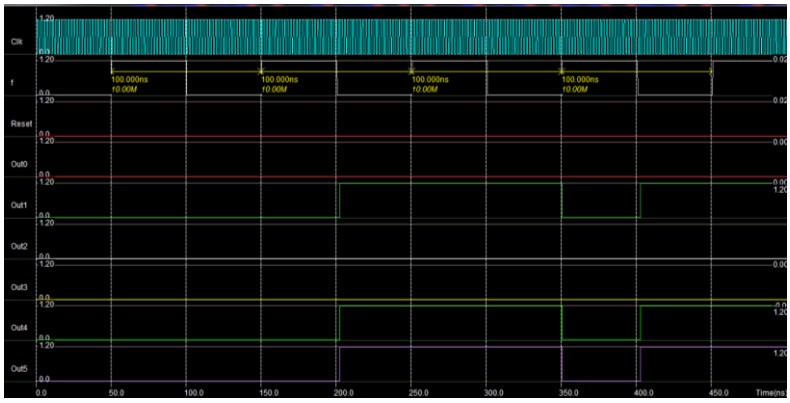

Figure4. *Simulation of the frequency meter for 6-stage counter and clock frequency 0.5 GHz*

Figure 5 shows dependency of power consumption P of frequency meter on the clock oscillator frequency F_{Clk} at the measurable frequency F = 10 MHz.

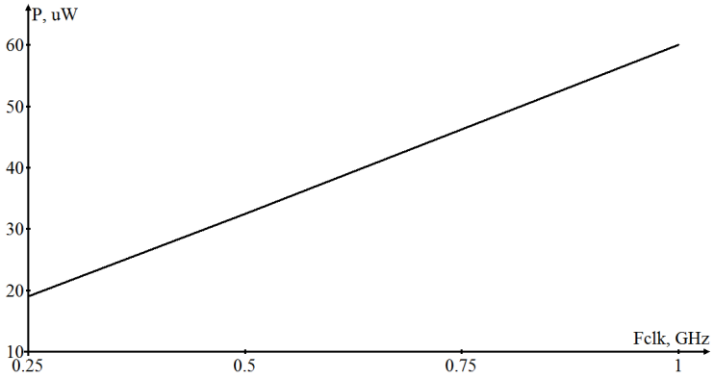

Figure5. *Dependence of power consumption on clock frequency at measurable frequency 10 MHz*

Dependences of minimal F_{min} and maximal F_{max} measurable frequencies on the number of stages n at different clock frequencies are shown in Figure 6. It follows from the figure that with increasing of the number of counter stages n the minimum measurable frequency F_{min} decreases. This broadens the measuring range of the frequency meter and in addition increases accuracy of the measurement. The increase of clock frequency also enlarges measuring range but leads to significant rising of the power consumption. Therefore choice of number of counter stages n and clock frequency F_{Clk} totally depends on requirements to the measurable frequencies range F_{min} - F_{max}.

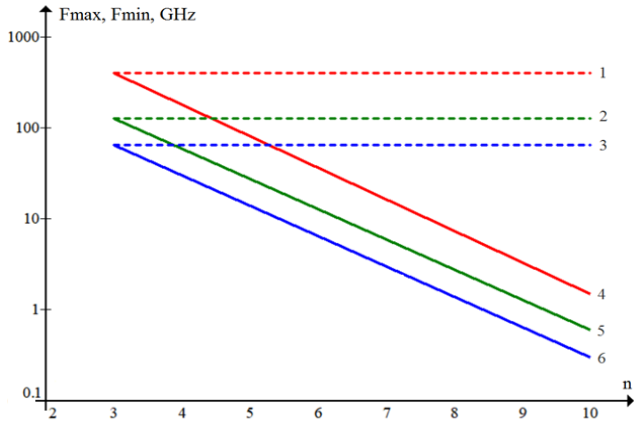

Figure6. *Dependences of F_{min} and F_{max} on number of stages n at different clock frequencies (F_{max}: 1 – at F_{Clk} = 1 GHz, 2 – at F_{Clk} = 0.5 GHz, 3 – at F_{Clk} = 0.25 GHz; F_{min}: 4 – at F_{Clk} = 1 GHz, 5 – at F_{Clk} = 0.5 GHz, 6 – at F_{Clk} = 0.25 GHz)*

4. CONCLUSION

The design of frequency meter unit for low-power systems is presented in this work. The schematic circuit, the layout and the simulation results are considered. The dependencies of power consumed by frequency meter on clock oscillator frequency as well as dependencies of the measurable frequencies range on the number of counter stages were obtained. Feature of the proposed frequency meter is opportunity of its implementation in the integrated-circuit form as the component of low-power detectors, micromechanical sensors and other devices in which the conversion of the signal frequency to the binary code corresponding to this signal is required.

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