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Comprehensive Analysis of Discontinuous Space Vector PWM Techniques for a Five-Phase Voltage Source Inverter

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Abstract: *This paper develops discontinuous space vector PWM (DPWM) technique for a five-phase voltage source inverter (VSI). Space vector model of a five-phase VSI shows that there exist 32 space vectors with three different lengths forming three concentric decagons. Application of outer most and middle set of space vectors to implement Space vector PWM yield nearly sinusoidal output. Thus the proposed DPWM utilises the same set of space vectors to implement the modulation techniques. Performance is evaluated in terms of total harmonic distortion and weighted total harmonic distortion in output phase voltages. A significant reduction in switching losses is observed. The simulation results are provided to validate the concept.*

1. INTRODUCTION

Multi-phase motor drives have gained much popularity in recent years and a number of research papers have been published. The main reason is the inherent advantages offered by multi-phase motors such as reduction in the amplitude and increase in the frequency of torque pulsation, reduction in the rotor current harmonics, reduction in the dc link current harmonics, reduction in the current per phase without increasing the voltage per phase leading and increasing the torque per ampere for the same volume machine. Keeping in view these advantages the application of multi-phase motors are coming up mainly in high power ranges such as ship propulsion, electric and hybrid vehicles, aircraft fuel pump applications etc. A review on multi-phase motor drives is available in [1,2]. Multi-phase motors need invariably some sort of power electronic converter for their supply as phases more than three is not readily available from the grid. The most common choice is a multi-phase voltage source inverter. There are mainly two methods of controlling the output voltage and frequency of inverters namely; square wave mode and pulse width modulation mode. A number of PWM techniques are available to control a three-phase VSI [3, 4]. However, Space Vector Pulse Width Modulation (SVPWM) has become the most popular method because of the easiness of digital implementation and better DC bus utilisation, when compared to the ramp-comparison sinusoidal PWM method. Another PWM method known as Discontinuous PWM is widely used because it offers reduced number of switching and consequently reduced switching losses. This aspect becomes extremely important when dealing with high power drive system, as even a small saving in switching losses means a large amount of overall power saving and thus enhanced energy efficiency of motors.

In principle, there is a lot of flexibility available in choosing the proper space vector combination for implementing space vector PWM for a multi-phase VSI. Space vector PWM technique for a five-phase VSI is illustrated in [5-10], where continuous mode is considered. This paper takes up issue of space vector PWM for a five-phase VSI in discontinuous mode. It is shown that the number of switching and consequently the switching losses can be greatly reduced by tiding one or more inverter legs to either positive or negative DC bus. This is termed as discontinuous space vector PWM which is developed for a five-phase VSI in this paper. Discontinuous space vector PWM is also available for a five-phase VSI in [11] where natural extension of three-phase discontinuous PWM was done and only large length vectors were used. Although the maximum possible fundamental output is high equal to 0.6115 p.u. but the output contain low-order harmonics. The switching is reduced by 40% compared to the continuous SVPWM. This paper utilises large and medium length space vectors to implement discontinuous SVPWM, providing sinusoidal output phase voltages. Similar discontinuous space vector PWM techniques are available in [12]. However, paper does not provide detail of the common mode voltage and other aspect of the PWM. In contrast this paper illustrates leg voltages, common mode voltages and the amount of reduction in switching due to each scheme. Moreover, two

novel methods are proposed in this paper, which yield better results compared to the existing schemes. The simulation results are provided to support the findings.

2. MODELING OF A FIVE-PHASE VSI

Power circuit topology of a five-phase VSI is shown in Fig.1. The inverter input DC voltage is regarded further on as being constant. The load is taken as star connected and the inverter output phase voltages are denoted in Fig.1 with lower case symbol *(a,b,c,d,e)*, while the leg voltages have symbols in capital letters *(A,B,C,D,E).* The model of five-phase VSI is developed in space vector form in [13], assuming an ideal commutation and zero forward voltage drop. A brief review is presented here.

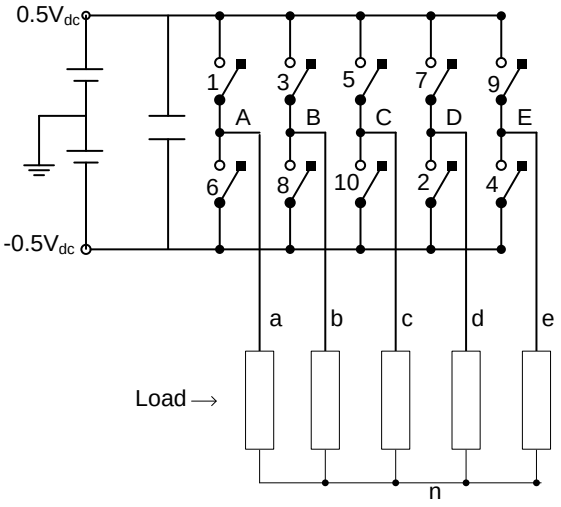


Fig1. *Power circuit of a Five-phase voltage source inverter*

There are ten switching devices and only five of them are independent, as the operation of two power switches of the same leg is complimentary. The combination of these five switching states gives out thirty two (32) space voltage vectors. Out of thirty two space vectors thirty are active vectors and two zero vectors. At any instant of time, the inverter can produce only one space vector.

The relationship between the machine's phase-to-neutral voltages and inverter leg voltages are given with

$$\begin{aligned} v_a &= (4/5)v_A - (1/5)(v_B + v_C + v_D + v_E) \\ v_b &= (4/5)v_B - (1/5)(v_A + v_C + v_D + v_E) \\ v_c &= (4/5)v_C - (1/5)(v_A + v_B + v_D + v_E) \\ v_d &= (4/5)v_D - (1/5)(v_A + v_B + v_C + v_E) \\ v_e &= (4/5)v_E - (1/5)(v_A + v_B + v_C + v_D) \end{aligned} \quad (1)$$

where the inverter leg voltages take the value of ± 0.5 V_{DC}. As noted, lower case letters in indices define phase-to-neutral voltages.

Space vector of phase voltages defined, using power variant transformation, as given in [14]:

$$\underline{v}_{dq} = \frac{2}{5}(v_a + \underline{a}v_b + \underline{a}^2 v_c + \underline{a}^{*2} v_d + \underline{a}^{*} v_e) \quad (2)$$

where$\underline{a}$ = exp(j2π/5), $\underline{a}^2$ = exp(j4π/5), $\underline{a}^*$ = exp(-j2π/5), $\underline{a}^{*2}$ = exp(-j4π/5) and * stands for a complex conjugate. The phase voltage space vectors thus obtained in *d-q* plane are shown in Fig.2. Since it is a five-phase system, transformation is further done to obtain space vectors in *x-y* plane using equation (3) and the resulting space vectors are shown in Fig. 3.

$$\underline{v}_{xy} = \frac{2}{5}(v_a + \underline{a}^2 v_b + \underline{a}^4 v_c + \underline{a}^6 v_d + \underline{a}^8 v_e) \quad (3)$$

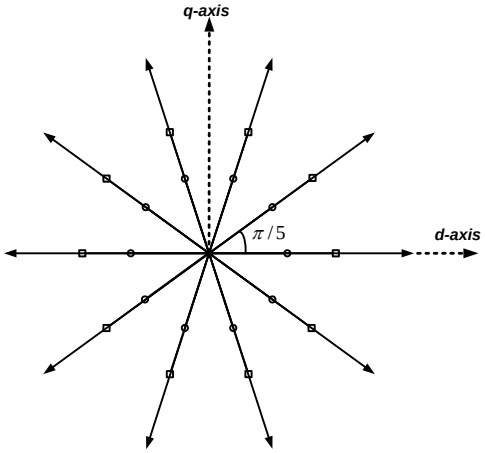


Fig2. *Phase voltage Space vector representation of all the thirty two states (zero vectors at origin)*

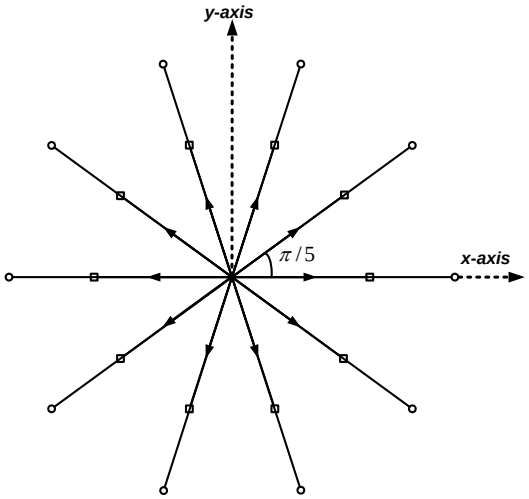


Fig3. *Phase voltage space vectors in x-y plane.*

It can be seen from Fig. 2 that the outer decagon space vectors of the *d-q* plane map into the inner decagon of the *x-y* plane (Fig. 3), the innermost decagon of *d-q* plane forms the outer decagon of the *x-y* plane, while the middle decagon space vectors map into the same region. Further, it is observed from the above mapping that the phase sequence *a,b,c,d,e* of the *d-q* plane corresponds to *a,c,e,b,d* sequence of the *x-y* plane.

3. CONTINUOUS SPACE VECTOR PWM SCHEMES FOR A FIVE-PHASE VSI

The purpose here is to generate sinusoidal output phase voltages using space vector PWM. Application of two neighbouring medium active space vectors together with two large active space vectors in each switching period makes it possible to maintain zero average value in the second plane [5-10] and consequently providing sinusoidal output. Use of four active space vectors per switching period requires calculation of four application times or dwell times, labelled here $T_{al}, T_{bl}, T_{am}, T_{bm}$. The expressions used for calculation of dwell times of various space vector are [5-6];

$$T_{al} = T_a \frac{|\underline{v}_l|}{|\underline{v}_l| + |\underline{v}_m|} \qquad T_{am} = T_a \frac{|\underline{v}_m|}{|\underline{v}_l| + |\underline{v}_m|}$$

$$T_{bl} = T_b \frac{|\underline{v}_l|}{|\underline{v}_l| + |\underline{v}_m|} \qquad T_{bm} = T_b \frac{|\underline{v}_m|}{|\underline{v}_l| + |\underline{v}_m|} \tag{4}$$

$$T_o = T_s - T_{al} - T_{am} - T_{bl} - T_{bm}$$

Large vector length is

$$|\underline{v}_{al}| = |\underline{v}_{bl}| = |\underline{v}_{l}| = \frac{2}{5} V_{DC} 2\cos(\pi/5) \tag{5}$$

Corresponding medium vector length is

$$|\underline{v}_{am}| = |\underline{v}_{bm}| = |\underline{v}_{m}| = \frac{2}{5} V_{DC} \tag{6}$$

Where

$$T_a = \frac{|\underline{v}_s^*| \sin(k\pi/5 - \alpha)}{|\underline{v}_l| \sin(k\pi/5)} T_s \tag{7}$$

$$T_b = \frac{|\underline{v}_s^*| \sin(\alpha - (k-1)\pi/5)}{|\underline{v}_l| \sin(k\pi/5)} T_s \tag{8}$$

This method divides the total vector dwell times to their respective lengths. This is in essence allocates 61.8% more dwell times to large space vectors compared to medium space vectors thus satisfying the constraints of producing zero average voltage in the *x-y* plane. This can be more clearly seen from Fig. 4.

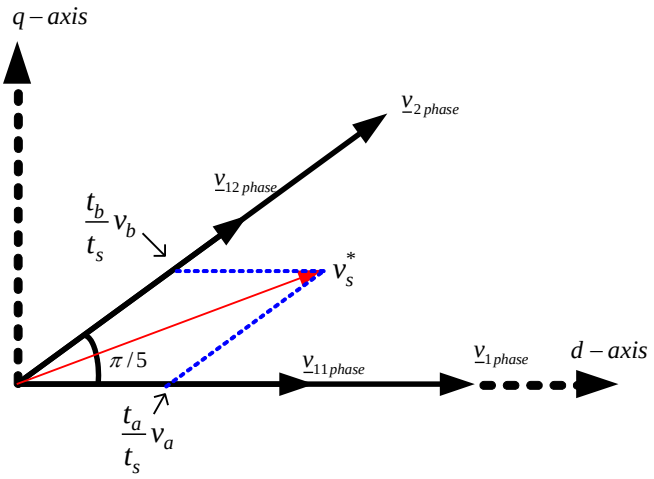


Fig4. *Principle of calculation of vector application times (d-q plane)*

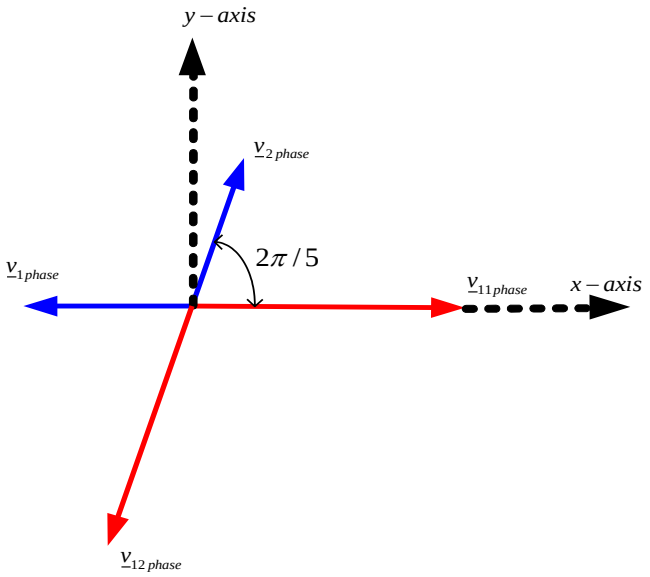


Fig5. *Principle of calculation of vector application times(x-y plane)*

It is seen from Fig. 4 that the vectors in *x-y* plane are in such a position to cancel each other by using the dwell time equations (4). The application of active and zero space vectors are arranged in such a way as to obtain a symmetrical SVPWM. The space vector disposition in sector I is illustrated in Fig. 5. Switching pattern is a symmetrical PWM with two commutations per each inverter leg. The space vectors are applied in odd sectors using sequence $[\underline{v}_0, \underline{v}_{al}, \underline{v}_{bm}, \underline{v}_{am}, \underline{v}_{bl}, \underline{v}_{31}, \underline{v}_{bl}, \underline{v}_{am}, \underline{v}_{bm}, \underline{v}_{al}, \underline{v}_0,]$, while the sequence is $[\underline{v}_0, \underline{v}_{bl}, \underline{v}_{am}, \underline{v}_{bm}, \underline{v}_{al}, \underline{v}_{31}, \underline{v}_{al}, \underline{v}_{bm}, \underline{v}_{am}, \underline{v}_{bl}, \underline{v}_0]$ in even sectors. It can be easily observed from equation (4) that the zero vector application time remains positive for $0 \le \left|v_s^*\right| \le 0.5257 V_{dc}$. Thus the output phase voltage from a VSI using this Space vector PWM scheme is $0.5257 V_{dc}$. The sequence of vectors applied and corresponding switching pattern for sector 1 is shown in Fig. 6 where states of five inverter legs take values of -0.5*Vdc* and +0.5*Vdc* (referencing to mid-point of the dc supply is applied) and the five traces illustrate, from top to bottom, legs A,B,C,D and E, respectively.

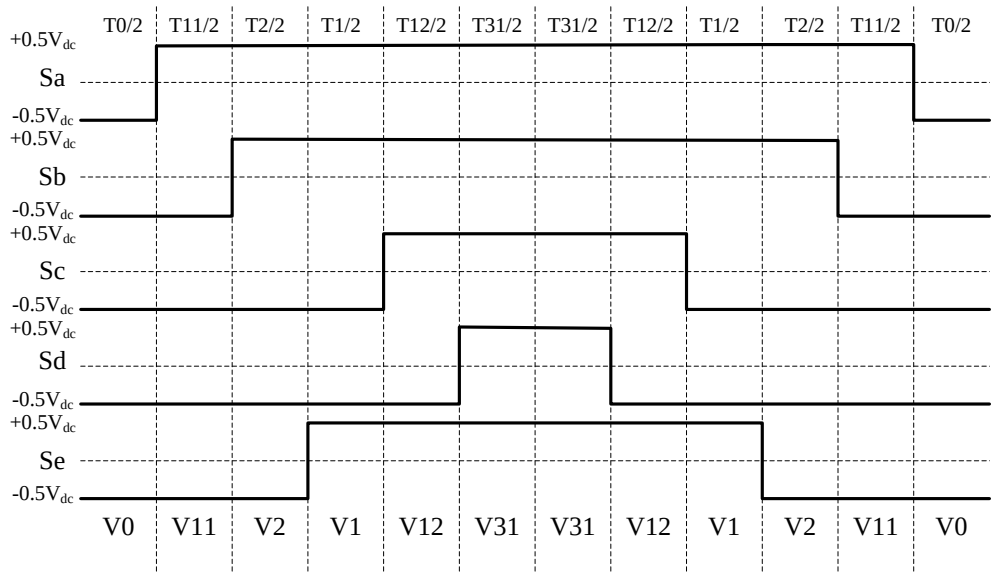


Fig6. *Switching waveform for sector 1 using large and medium vectors.*

4. PROPOSED DISCONTINUOUS SPACE VECTOR PWM

It is possible to move the position of the active voltage pulses within the half switching interval, to eliminate one zero output voltage pulse. Modulation strategies using this concept are termed as discontinuous modulation. This method causes one or more inverter leg to tie to either positive or negative dc bus. This scheme is mainly important for high power applications where switching losses are considerable. Six different Discontinuous space vector PWM techniques are proposed and presented in this section. However, all the schemes essentially just rearrange the placement of the zero space voltage vectors within each half carrier or carrier interval. The method where $t_{31}(11111)$ is kept zero for the complete fundamental cycle is termed as DPWMMIN and the method where $t_0(00000)$ is kept zero for one fundamental cycle is termed as DPWMMAX. Rest of the four methods splits the sectors and arranges the zero space vectors in various fashions are termed as DPWM0, DPWM1, DPWM2 and DPWM3. The time of application of various space vectors are still governed by equation 4. The fundamental output voltage magnitude and the nature of phase voltage waveforms remains sinusoidal as that of continuous SVPWM.

The switching waveforms for different discontinuous PWM methods are shown in Fig. 7.

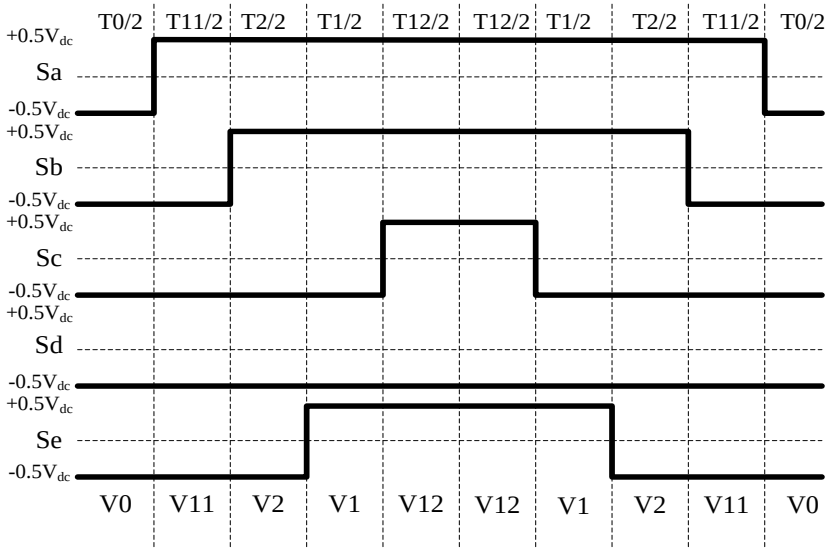


Fig7a. *Switching waveform for sector 1 using large and medium vectors for DPWMMIN*

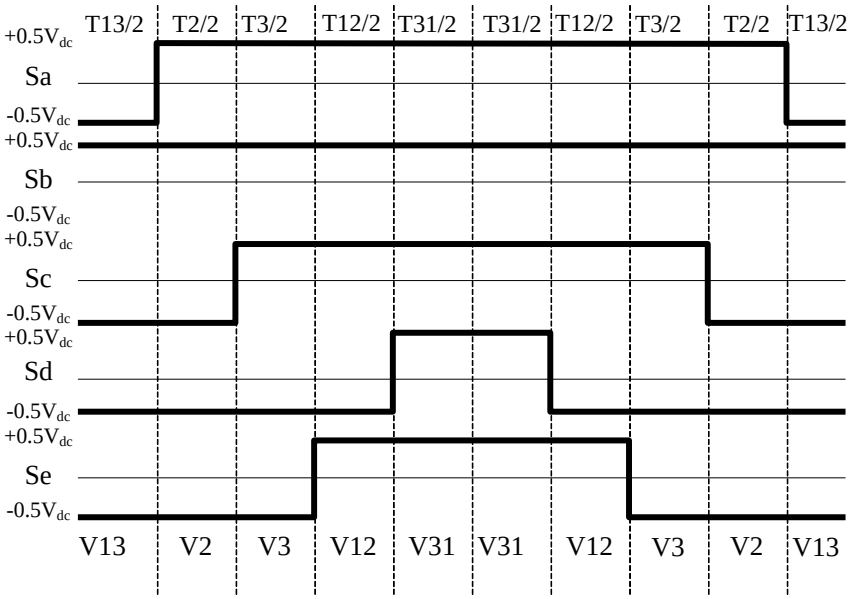
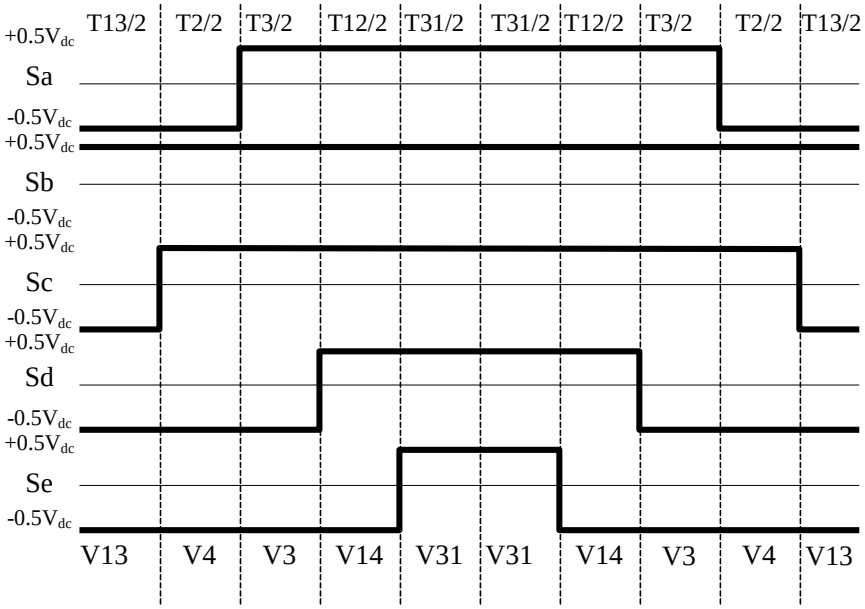
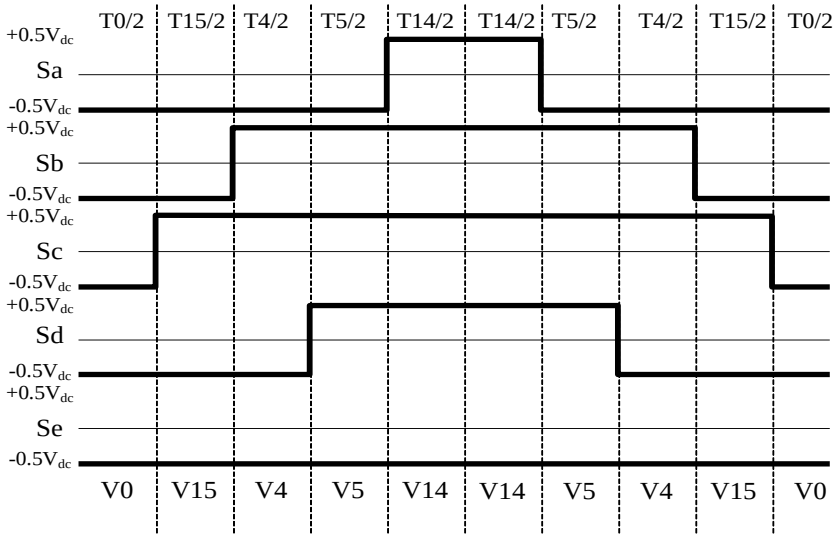


Fig7b. *Switching waveform for sector 2 using large and medium vectors for DPWMMAX*

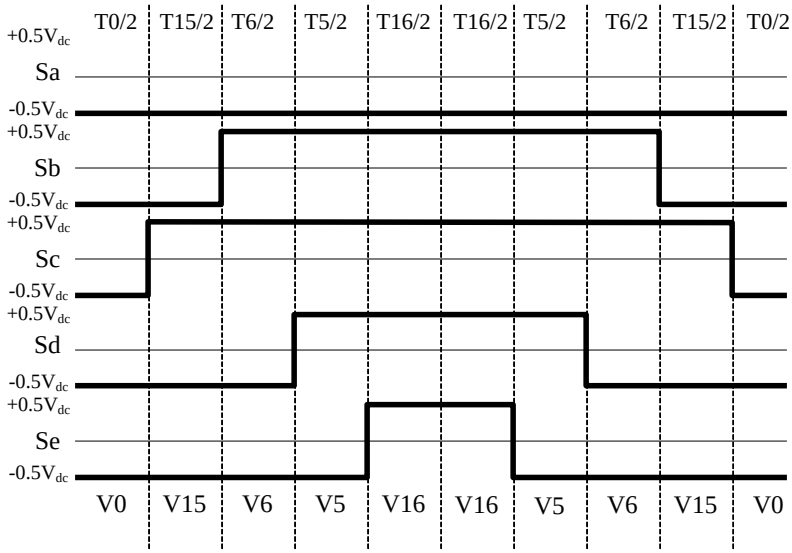


(i)

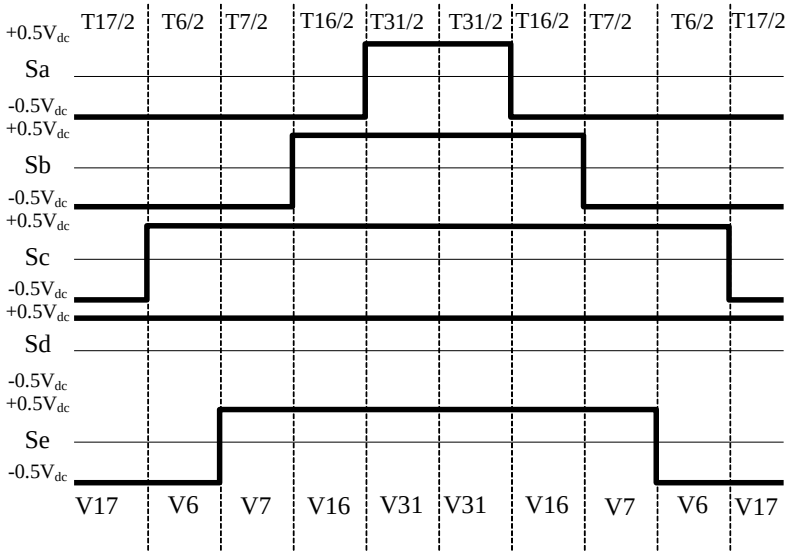


(ii)

Fig7c. *Switching waveform for (i) sector 3 (ii) Sector 4 using large and medium vectors for DPWM0.*



(i)



(ii)

Fig7d. *Switching waveform for (i) sector 5 (ii) sector 6 using large and medium vectors for DPWM1.*

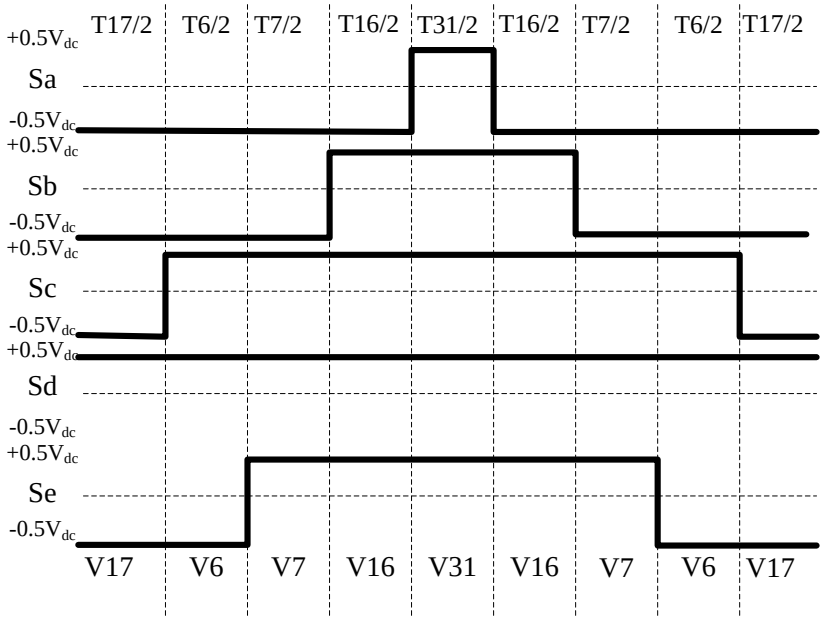


Fig7e. *Switching waveform for sector 6 using large and medium vectors for DPWM2.*

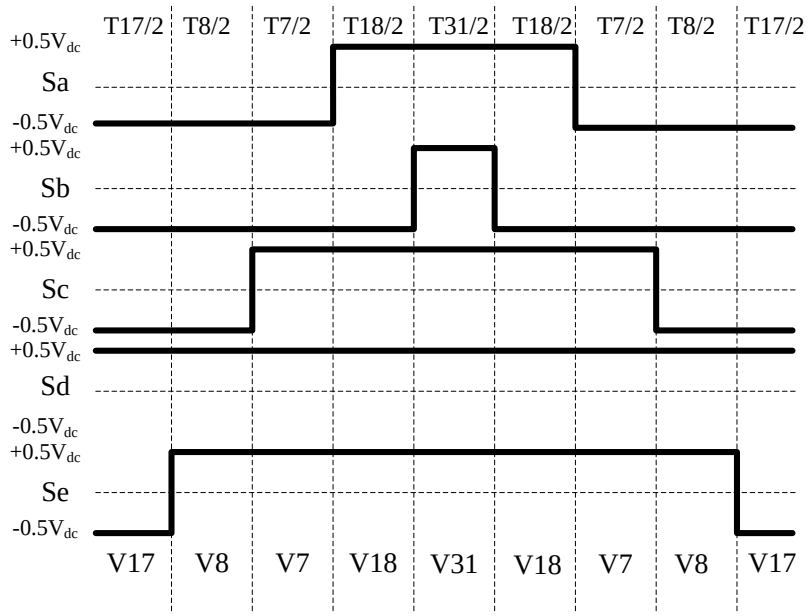
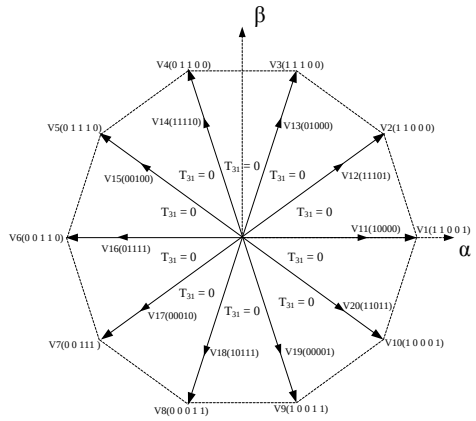
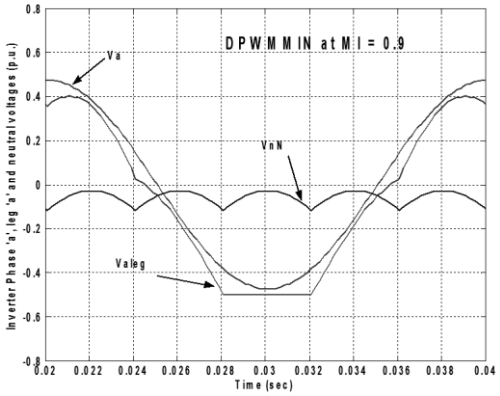


Fig7f. *Switching waveform for sector 7 using large and medium vectors for DPWM3*

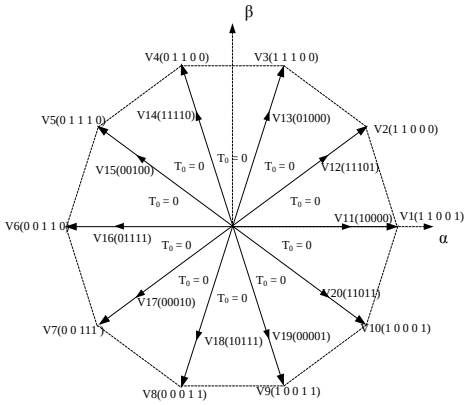
It is seen from Fig. 7 that one leg is tied to either positive or negative dc bus so no switching takes place in that leg. There are ten sectors and ten switches in a five-phase VSI thus one leg remains idle in two sectors i.e. for 72°, upper switch of a leg is inoperative in one sector and lower one in other one sector. In DPWMMIN each leg is tied to the DC bus for two subsequent sectors. For instance in DPWM0 upper switch of leg D is tied to lower dc bus in sector 1 and the upper switch of the same leg is tied to the upper dc bus in sector 6. Thus the number of switching is now reduced by one fifth compared to their continuous counterpart and consequently a corresponding reduction in switching losses.

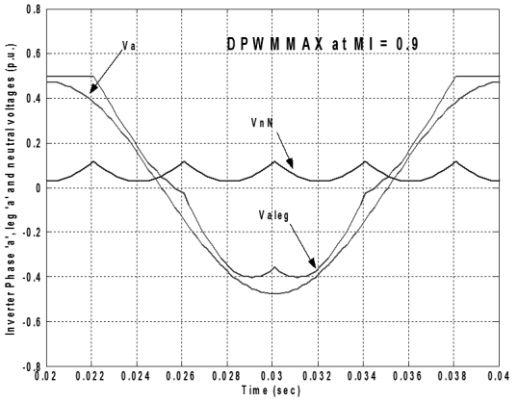
All the proposed schemes are simulated using Matlab/Simulink and the resulting waveforms are shown in Fig 8. Part (a) of Fig 8 shows the placement of zero vectors in different sectors and part (b) of Fig 8 shows the waveforms for each schemes where $V_{a\,leg}$ (average leg voltage), V_a (average phase voltage), V_{nN} (average voltage between neutral points) called common mode voltage. The switching frequency is taken as 5 kHZ and the fundamental frequency is chosen as 50 Hz. The reference input is varied from 0 to the maximum obtainable (0.5257 (p.u.)).



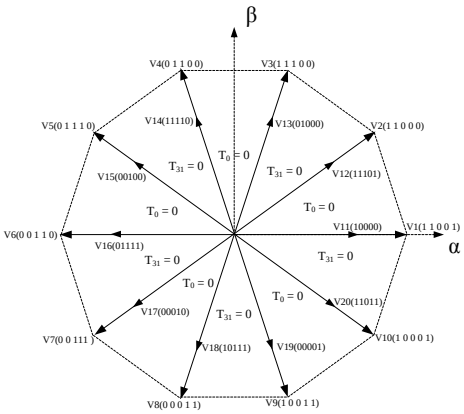


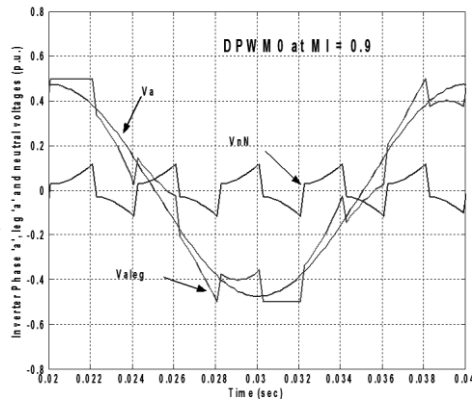
DPWMMIN



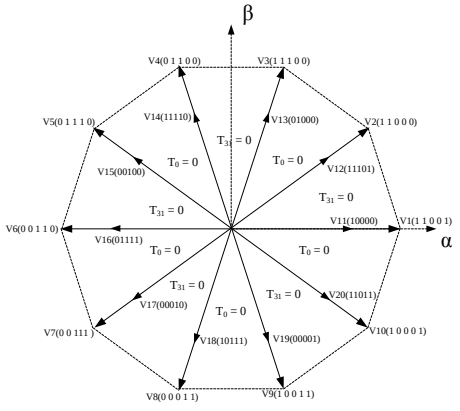


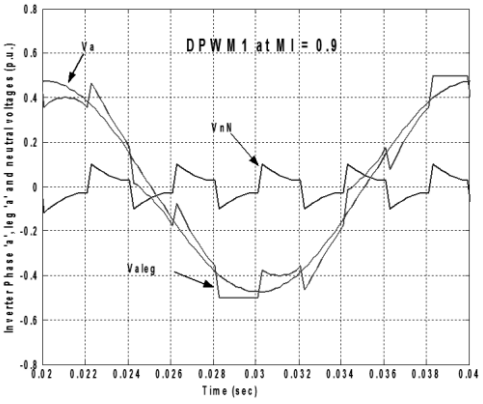
DPWMMAX



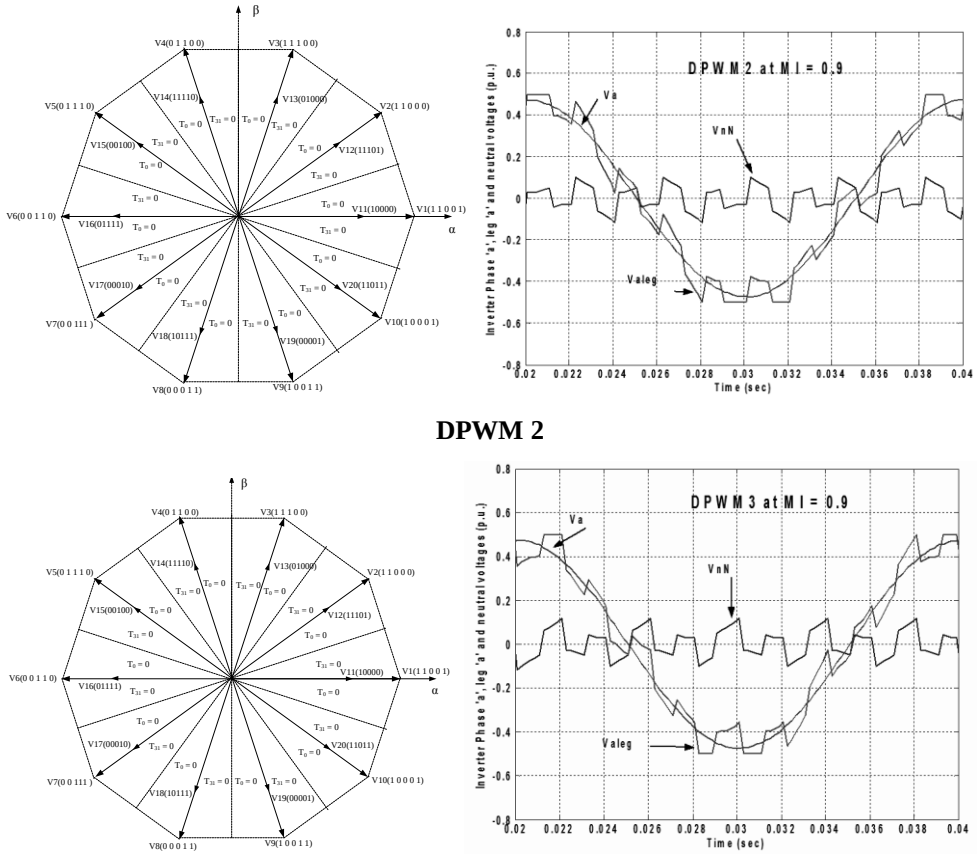


DPWM 0





DPWM 1



DPWM 2

DPWM 3

Fig8. *Wave forms for different DSVPWM schemes.*

Basic schemes designated as DPMWMMIN and DWPWMMAX tied each leg to negative dc rail and positive dc rail, respectively and thus the name MIN and Max are given to them. These schemes are thus not recommended for use as they may damage either the lower or upper switches of VSI. To avoid this situation three more techniques namely DPWM0, DPWM1 and DPWM2 are suggested in which DPWMMIN and DPWMMAX are applied alternatively in each sector so that each leg can be kept inoperative alternately providing a symmetric switching. Each of the three methods proposed here are suitable to feed different types of loads. It can be observed from Fig. 8, for DPWM0 that the discontinuous period is 18° lagging the phase voltage and thus the most suitable load will be the one operating at $\cos(18)$ power factor leading. This is because of the fact that in the range of discontinuous period the current is maximum and the number of switching is minimum offering lower switching losses. Similarly for DPWM1 the suitable load power factor is $\cos(18)$ lagging. It is further seen for DPWM1 and DPWM2 the discontinuity is splitted in two parts and thus two different loads may be catered are $\cos(9), \cos(24)$ power factor lagging and or leading.

Simulation is once again carried out for different loading conditions. The load considered is standard series RLC type of load whose transfer function is given by equations (9) and the resulting average voltage, average current and leg voltages are shown in Fig. 9.

$$TransferFunction = \frac{(1/L)s}{s^2 + (R/L)s + 1/LC} \tag{9}$$

Keeping R = 1 ohm and *Xc* = 1 ohm,

$$TransferFunctionfor\ 9\deg leading = \frac{(373.28119)s}{s^2 + (373.28119)s + 117273.3896} \tag{9a}$$

$$TransferFunctionfor\ 9\deg lagging = \frac{(271.204673)s}{s^2 + (271.204673)s + 85204.10713} \tag{9b}$$

$$Transfer Function for\ 18\deg leading = \frac{(465.3657)s}{s^2 + (465.3657)s + 146203.5093} \tag{9c}$$

$$Transfer Function for\ 18\deg lagging = \frac{(237.1157)s}{s^2 + (237.1157)s + 74494.4087} \tag{9d}$$

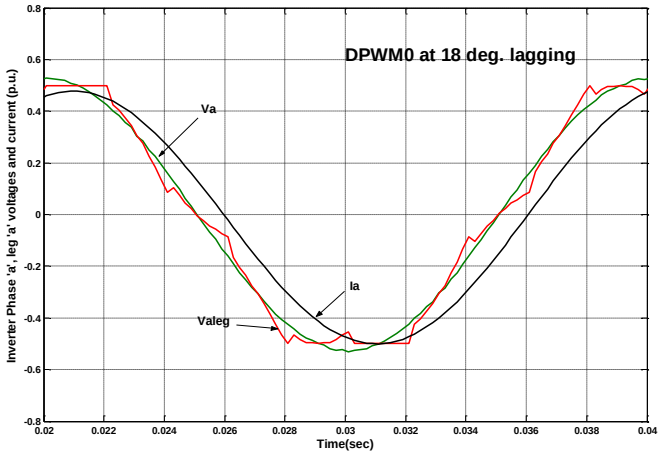


Fig9a. *Average leg and phase voltages and current for 18 degree lagging load for DPWM0.*

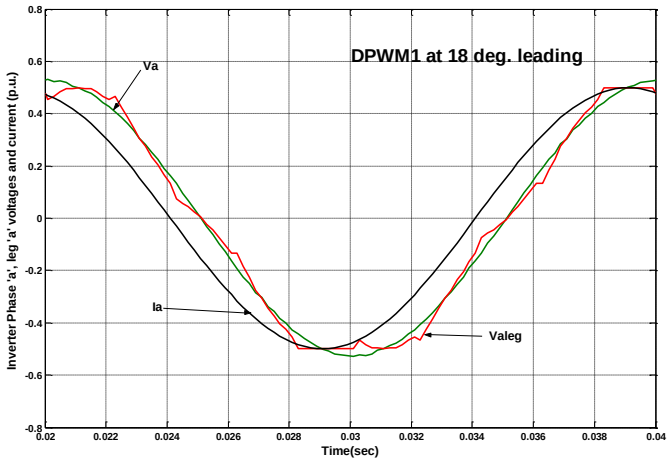


Fig9b. *Average leg and phase voltages and current for 18 degree leading load for DPWM1.*

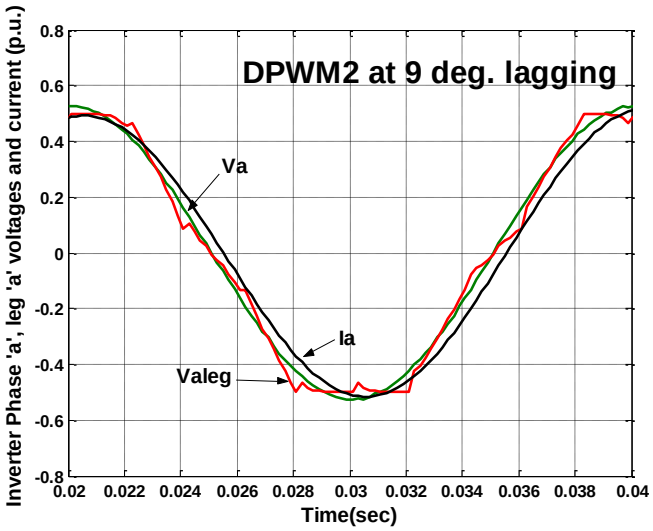


Fig9c. *Average leg and phase voltages and current for 9 degree lagging load for DPWM2.*

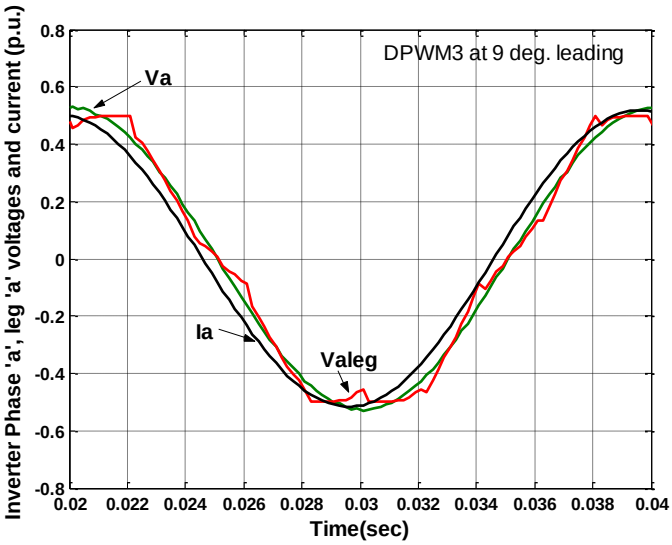


Fig9d. *Average leg and phase voltages and current for 9 degree leading load for DPWM3.*

It is seen from Fig. 9 that the load profile exactly matches the requirement of the modulator (current peak coincides with the discontinuous region of the leg voltages) and thus the switching losses in these cases are minimum.

5. GENERALIZED DISCONTINUOUS SVPWM

A generalised discontinuous Space vector PWM was suggested in [15] for a three-phase VSI. The same concept is extended here for a five-phase VSI. A generalised neutral or common mode voltage is generated which is then injected into the reference voltage to obtain a set of modulating signals. These modulating signals are then compared with high frequency triangular wave to generate the gate drive signals. Although this is a carrier-based PWM method but it produces the output of the similar quality to that of the space vector PWM. The method can be explained using Fig. 10. Modulator phase angle is denoted by α and is measured from the intersection point of the two reference waveat $\omega t = \pi/5$. The common mode voltage shown as shaded portion in Fig. 10 is obtained as;

$$v_{nN} = \text{sgn}(v_a, v_b, v_c, v_d, v_e) * 0.5V_{dc} - \max(v_a, v_b, v_c, v_d, v_e) \tag{10}$$

At first the maximum reference voltage is identified and then the difference between the available dc bus voltage $(0.5V_{dc})$ and the maximum of the reference yield common mode voltage. The control range of $\alpha \rightarrow [0 - \pi/5]$ to keep the operation of modulator in the linear range.

6. PERFORMANCE EVALUATION

Two parameters are taken in consideration for performance evaluation of the proposed DSVPWM methods namely Total Harmonic Distortion (THD) and Weighted Total Harmonic Distortion (WTHD) and are defined in [3] by equations (11) and (12),

$$\text{THD} = \sqrt{\sum_{n=3,5,7..}^{\infty} \left(\frac{V_n}{V_1}\right)^2} \tag{11}$$

$$\text{WTHD} = \frac{THD}{(V_1/\omega_1 L)} = \frac{\sqrt{\sum_{n=2}^{\infty} \left(\frac{Vn}{n}\right)^2}}{V_1} \tag{12}$$

Where V_n represents n^{th} order harmonic component and V_1 represent fundamental output phase voltages. The lower order harmonic contents (upto 25^{th} order) are considered for calculation of THD and WTHD. The simulation is carried out to determine these performance indices for the complete range of the modulation index. The resulting THD and WTHD are shown in Fig. 11.

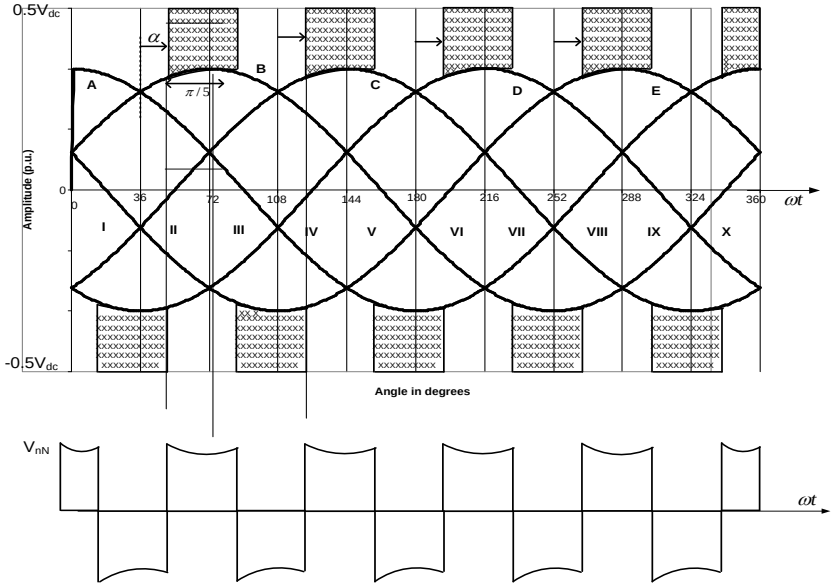


Fig10. *Generalised Discontinuous PWM method*

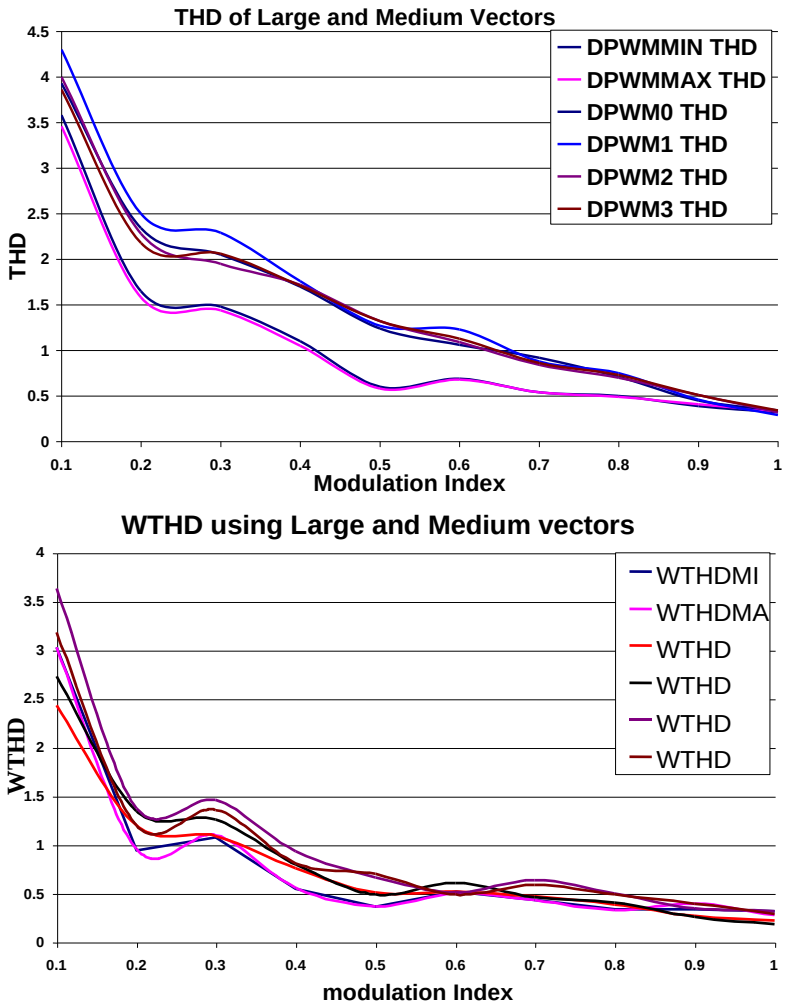


Fig11. *THD and WTHD for various modulation index.*

It is seen from the Fig. 11 that at lower modulation index the best method is DPWMAX while at high modulation index DPWM1 offers minimum THD and WTHD. To further illustrate the variation of THD and WTHD two plots are shown in Fig. 12, one at 0.3 modulation index and other at unity modulation index.

At Modulation Index = 0.3

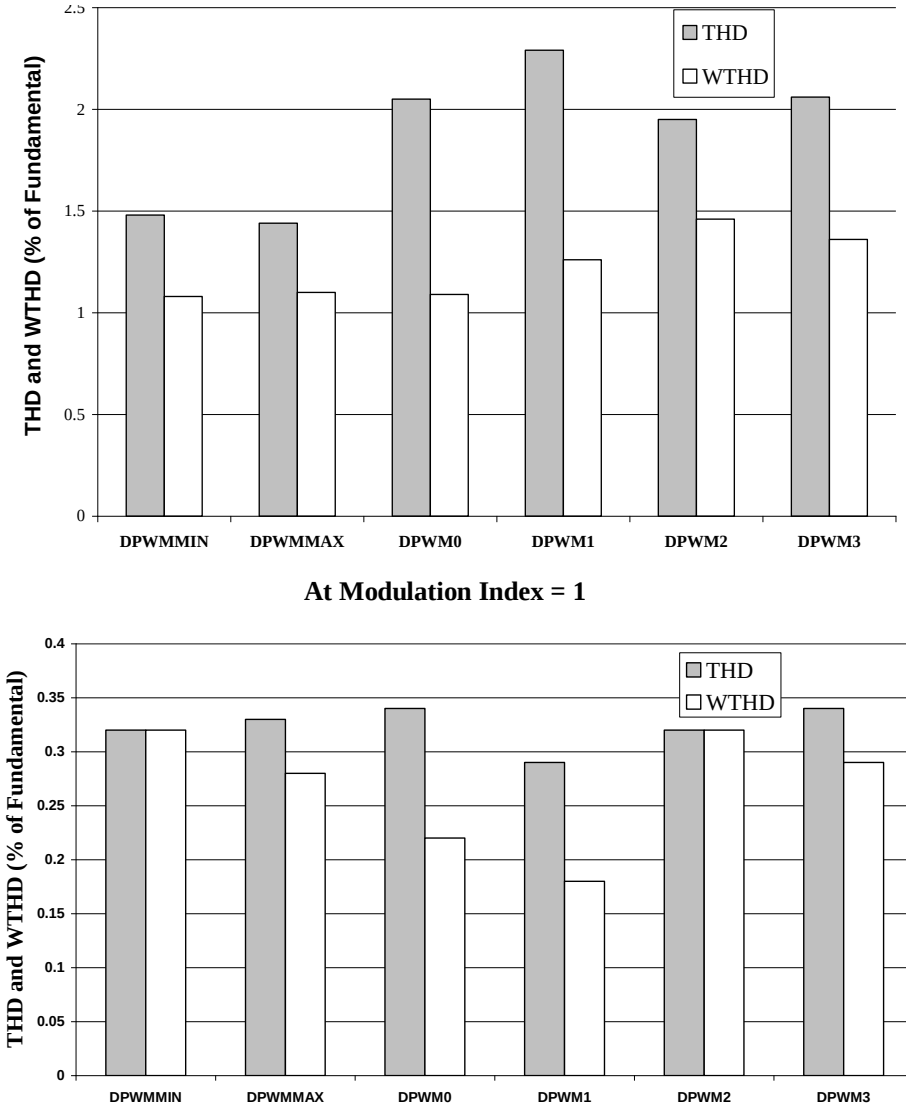


Fig12. *THD and WTHD at modulation index 0.3 and 1 for different DPWM method.*

It can further be seen from Fig. 12 that at low modulation index the THD and WTHD of DPWMMAX is lower than all the schemes and DPWM1 has highest THD. Since the DPWMMAX cannot be employed for implementation purposes, thus the next best scheme is DPWM2. At high modulation index the value of THD and WTHD is smaller compared to the value at lower modulation index, which implies that the output voltage is very near to the sinusoidal. DPWM1 has lowest THD and DPWM0and DPWM3 has highest THD at high modulation index.

7. EXPERIMENTAL INVESTIGATION

A Five-phase voltage source inverter is developed using intelligent power module from VI Micro systems, Chennai. Texas Instrument DSP TMS320F2812 is used as the processor to implement the control algorithm. Since this DSP may coded in C or C++, it is more user friendly and they have dedicated 16 hardware PINS to generate the desired PWM signals. The PWM circuits associated with compare units make it possible to generate upto eight PWM output channels (per Event Manger) with programmable dead band and polarity. This DSP is specifically meant for use in motor drive purposes and it can control upto 8-phase two-level inverter. The control code is written in C++ language in Code composer studio 3.3 which runs in a PC. The control signal generated by PC is transferred to the DSP board through RS 232 cable connected in parallel printer port of the PC. The DSP board is connected to the Power Module through dedicated control cable. The DSP interfacing circuit along with required A/D and D/A converter is built on the DSP board itself procured from VI Micro systems. The complete experimental set up is shown in Fig. 13.

Fig13. *Five-phase experimental set up.*

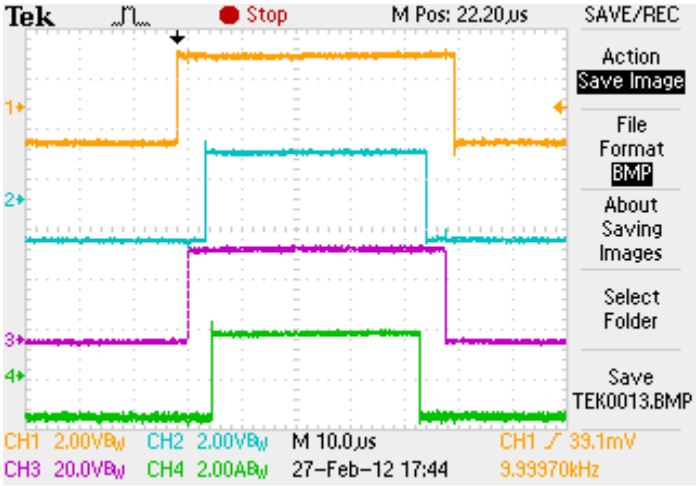


Fig14. *Switching pattern for the proposed PWM*

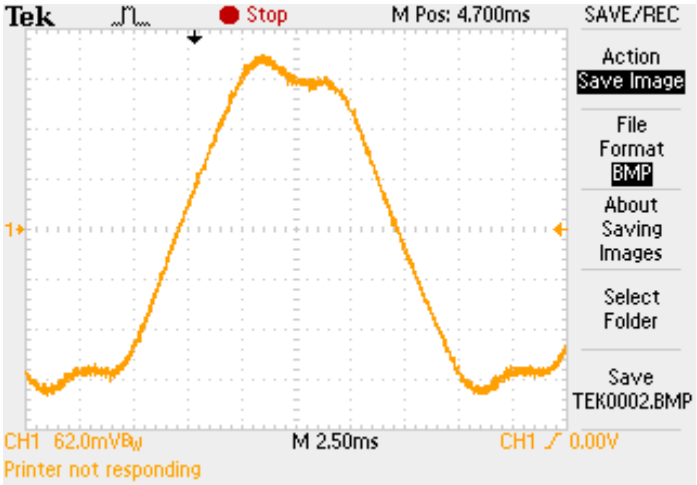


Fig15. *Leg voltage for DPWMMIN*

8. CONCLUSION

The paper present a PWM technique termed as Discontinuous Space Vector PWM for a five-phase voltage source inverter. There exist two methods of SVPWM in a five-phase VSI, one utilises only large space vector set while the other utilises both large and medium vector sets. This paper utilises large and medium vectors to synthesise the input reference in discontinuous mode. This method of PWM offers a reduction in overall number of switching and consequently switching losses.

DSVPWM utilising large and medium space vector is seen to reduce the number of switching to 1/5th and consequently the switching losses. Alternatively the inverter switching frequency can be enhanced keeping the same inverter losses. Six different schemes are proposed and presented. The analysis is done on the basis of two performance indices namely THD and WTHD. It can be concluded that the DPWMMAX provide lowest THD and WTHD for low modulation index. However, this method is not recommended for practical implementation as this may shorten the life of inverter. DPWM2 offers the next best result and thus it may be used for implementation. At high modulation index DPWM1 is recommended for use. A generalised discontinuous PWM method is proposed based on triangle comparison method. This method is easy to implement, it will provide different DPWM schemes depending upon the modulation index. The viability of the proposed schemes is validated using simulation results.

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