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The Proposed Research Technology and Data Implementation Process for Prevention of Over-Voltage Failures in Adjustable Speed Drives Using DC Bus Voltage Clamp Method

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Abstract: *This paper investigates PWM and Long cable length effect on the voltage insulation components inside an adjustable speed drive (ASD). This paper shows that high potential voltage insulation issue may exist on various components inside the ASD and cause earlier failures under very long cable or multiple drive conditions. A dc bus voltage clamp circuit is proposed to reduce these voltage stresses. The effectiveness of this circuit is verified by simulation.*

Index Terms: *Adjustable speed drive (ASD), insulation, long cable, voltage clamp circuit.*

1. INTRODUCTION

Advances in power electronics technology has enabled the adjustable speed drives (ADS) to reach higher switching and improved controllability of voltage current and torque. The fast dv/dt PWM switching of the inverter device may reduce noise and these devices may induce high frequency ground leakage current, high shaft insulation voltage, and high levels of bearing current. Numerous References have discussed analyze these issues [1]–[11]. Chen and Lipo [1] pointed out that a net common-mode cur-rent flowing through three-phase stator windings to the axial direction produces a time-varying flux surrounding the motor shaft. This flux induces a shaft end-to-end voltage driving a circulating bearing current in turn. Reference [2]–[5] analyzed the PWM switching and cable length effect on bearing current, EMI emission, and motor insulation. In [4]–[12], various methods and topologies were proposed to reduce the effect of the PWM switching on motor insulation, EMI performance and bearing current effect; However, they cannot reduce the voltage stresses inside the ASD drive.

One simple assumption made from these references is that the common mode capacitance inside the drive is much higher than the common mode impedance external to the inverter. This is true for majority of applications. However, when an ASD is applied with very long cable or multiple parallel cables, common mode capacitance of the cable and motor may be comparable or even higher than the common mode capacitance inside the drive. Under this condition, high voltage stresses may be generated inside the drive.

Now a days, the physical sizes of the ASD drive and its high voltage components have been reduced. Typical ways of reducing drive size is to replace the bus bars with printed circuit board (PCB), to integrate high voltage component with low voltage circuitry, to shrink the component sizes, and to reduce or remove unnecessary components. All above optimizations may increase voltage stresses of these components and cause unexpected voltage failures.

This paper investigates the effects of PWM switching and long cable lengths on voltage stresses of different components inside the ASD.

2. METHODOLOGY

To analyse the voltage stresses, First to categorizes the high voltage components and analyze their voltage stresses of the component. It is found out that the voltage stresses of the component can be simplified by analyzing the voltage differences between dc bus terminals and the ground potential (GND). It is found out that several potential high voltage stresses operating conditions (much higher

than the dc bus voltage) may exist for some severe conditions. After that, a simple dc bus voltage clamp circuit is introduced to reduce the voltage stresses.

A. Voltage Stresses in Adjustable Speed Drive

❖ High Voltage Components and Their Voltage Stresses in ASD Drive

There are two types of high voltage components based on the use of low voltage control signal to control high voltage switching devices in adjustable speed drives.

- Common mode circuit
- Differential mode circuit

The first type of components are the main circuit components that transfer power from line to load side, including inverter IGBT, rectifier diode/SCR, dc link choke, dc bus capacitor, snubber capacitor, and etc. They are all located in the differential mode (DM) circuit and their voltage stresses are generally no higher than the dc bus voltage.

The second type of components provide protective separation between the control circuit and the main circuit, including opto-coupler, PCB, sensors, voltage/current transducer, switch mode power supply (SMPS) transformer, and etc. The high voltage (HV) sides of these components are either no higher than the positive bus or no lower than the negative bus.

❖ Differential Mode Voltage Between DC Bus Terminals to the GND

The voltage stresses between the ground and the dc bus terminals can be calculated by adding the common mode and differential mode components.

For the differential mode circuit, this voltage stresses can be approximated as half the dc bus voltage for a Y grounded system. Where

$$\text{Vpgpk\_DM} = \frac{Vdc}{2} \qquad \text{Vngpk\_DM} = -\frac{Vdc}{2} \qquad (1)$$

where Vpgpk_DM is the maximum voltage between positive dc bus and the GND in differential mode circuit, Vngpk_DM is the minimum voltage between negative bus voltage and the GND in differential mode circuit.

For a corner grounded system, the maximum voltage stresses between dc bus terminals to the GND can be as high as dc bus voltage between positive bus and the GND and as low as negative dc bus voltage between negative bus to the GND as shown in

$$\text{Vpgpk\_DM} = Vdc \qquad \text{Vngpk\_DM} = -Vdc \qquad (2)$$

❖ Common Mode Voltage Between DC Bus Terminals and the GND

For the common mode voltage, it is determined by the cable length, common mode capacitance of the ASD drive, and PWM switching frequency. This voltage can be much higher than the rated dc bus voltage for some cable and operating conditions as explained in the following sections. As a result, the common mode model of the cable and motor is simplified as a single L–C–R circuit.

❖ Voltage Stresses Analysis and the Capacitance Ratio Between ASD and the Load a Discontinuous Mode

The worst case common mode voltage stress in capacitor Cf generated by a single common mode voltage step of Vdc (zero speed) can be calculated as

$$\mathbf{V}\text{cmpk} = \frac{2Vdc\,.\,Ccmo}{Ccmo + 2\,.\,Cf} = \left(2 - \frac{4Cf}{Ccmo+2Cf}\right)\text{Vdc} \qquad (3)$$

where Cf is the common mode capacitor in dc link, the Ccmo is the equivalent common mode capacitor of the cable and motor.

For majority of the applications, common mode filter capacitor Cf is much higher than Ccmo. The peak common mode voltage stresses of Cf are low and the voltage potential of GND is between dc+ and dc−. The voltage stresses of the protective insulation components are low. For some special conditions where multiple cables or very long cables are associated, the total capacitance Ccmo may

be higher than common mode capacitance Cf . The peak voltage induced in the common mode capacitor will be increased to as high as twice the dc bus voltage. As a result, the voltage stresses of the protective separation component may be two times higher than the dc bus

- **Overall Stresses Adding DM and CM Voltages**

The worst case voltage stresses of between the dc bus to the GND adding differential mode voltage for Y grounded system can be expressed as

$$Vpg = Vpgpk\_DM + Vcmpk = (2.5 - \frac{4Cf}{Ccmo+2Cf})Vdc$$

$$Vpg = Vpgpk\_DM - Vcmpk = -(2.5 - \frac{4Cf}{Ccmo+2Cf})Vdc \quad 4$$

where, Vpg/Vng is the voltage stresses between dc+ /dc− and

GND, respectively

For corner grounded system, the worst case voltage stresses between the dc bus terminals to the GND adding differential mode voltage can be expressed as

$$Vpg = Vpgpk\_DM + Vcmpk = (3 - \frac{4Cf}{Ccmo+2Cf})Vdc$$

$$Vng = Vpgpk\_DM - Vcmpk = -(3 - \frac{4Cf}{Ccmo+2Cf})Vdc \quad 5$$

Theoretically, the maximum voltage stresses existed between dc bus terminals when the common mode capacitance *Cf* is 0 and the inverter operated at low speed. It can reach as high as 2.5 time of the dc bus voltage for Y grounded system and 3 time of the dc bus voltage at corner grounded system. However, this value is an ideal calculation by neglecting the damping of the output common mode circuit and the common mode capacitance of the power converter. Due to the conductor resistance and insulation resistance between cable and the ground, the peak voltage stress may never be able to reach this level.

3. PROPOSED VOLTAGE CLAMP METHOD

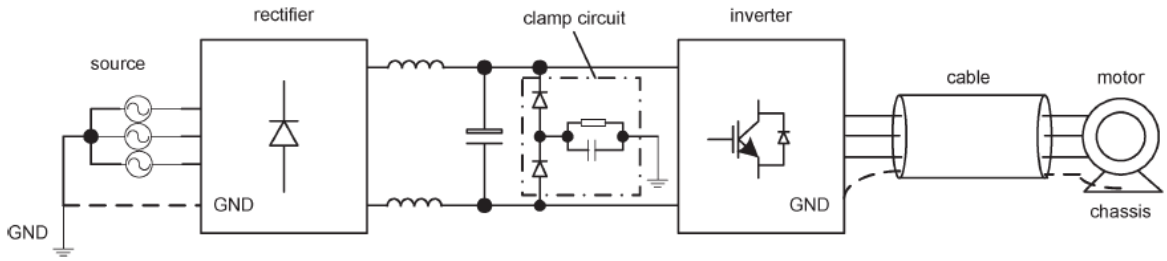

Fig 1. *Shows the proposed voltage clamp circuit for an ASD drive .It consists of three types of components.*

- Two diodes clamped between the neutral of the two diodes and the GND. The snubber capacitance is generally selected to be higher than the common mode capacitance of the cables and motors. The leakage inductance between the capacitor to the dc bus terminal should be designed as low as possible.
- A discharging resistor in parallel with the clamping Capacitor and grounded.

There are three operation modes of the clamp circuit.

- Standby Mode
- Clamping Mode
- Discharging Mode

Standby Mode:

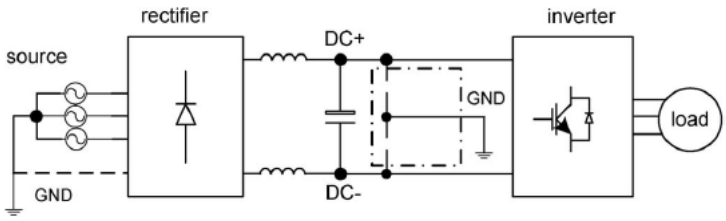

Fig.2a *Standby Mode*

During normal condition, the voltage of the GND is always lower than the dc+ and higher than dc−, both diodes are anti-biased. The voltage across the RC snubber circuit is zero as shown in Fig.2a

Clamping Mode:

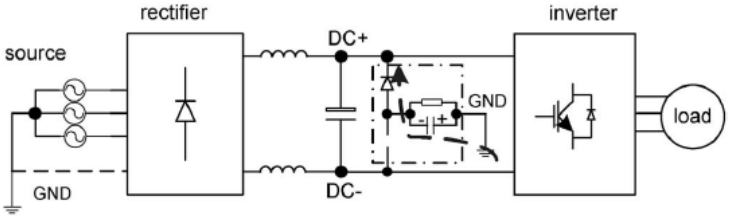

Fig.2b *clamping Mode*

If the GND is either higher than dc+ or lower than the dc−, one of the diode starts to conduct. The common mode energy will be transferred to the RC snubber circuit, since the capacitance of this snubber circuit is selected to be much higher than the overall cable and motor common mode capacitance.

The potential of the GND will be clamped to one of the two dc bus voltages (dc+ or dc−). Fig.2b shows a circuit diagram at this mode when Vgnd is higher than Vdc+. The voltage difference between GND and bus terminal is slightly higher than

Vdc = (Vdc+) − (Vdc−)

Discharging Mode:

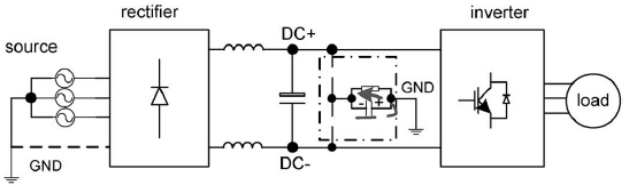

Fig.2c *Discharging Mode*

After the PWM switching transient is over, the GND potential is low than dc+ and higher than the dc−. Both diodes return to off condition. The energy of the snubber capacitor is now discharged by the snubber resistor. After all energies are discharged, the system goes back to standby mode. The voltage difference between GND and bus terminal is still less than

*V*dc =*V*dc+ − *V*dc−.

To guarantee that the system goes back to standby mode during each switching cycle, the time constants of the RC snubber can be selected as much lower than the PWM frequency. Since the resistor is only used to discharge the power, the leakage inductance of the resistor is not critical as well.

It should also be noted that the watt loss of the RC snubber resistor is proportional to the switching frequency of the inverter. The wattage of the resistor is much lower than the energy being charged/discharged by the inverter cable capacitance. While selecting the RC resistor, its wattage must be able to support the inverters to operate under the highest switching frequency.

The proposed method has the following advantages.

• It has the minimum number of components, only two diodes and a RC snubber circuit is needed.

• The voltage across the capacitor is zero majority of time, the voltage stresses on the clamped capacitor is much lower than other topologies.

• The circuit only starts to operate when the GND potential is higher than dc+ or lower dc−. The wattage losses of the discharging resistor can be much lower than any other circuit that operates all the time.

4. SIMULATION RESULT VERIFICATION

Several potential high voltage stress cases are studied in Simulation. During the study, the drive and motor data used are shown below.

ASD drive rating: 480 V/75 hp

Switching frequency: 4 kHz

Common mode capacitance: 0.1 uF or 0.001 uF

Cable length: 1200 ft shielded/AWG #2

Motor: 460 V/50 hp/59.6 Arms

The value of the clamp circuit components are:

Snubber capacitor: 5 uF

Snubber resistor: 86 Ω

Diode: 1200 V/10 A rated

1. Proposed without and with clamp ciricuit for a solid Y ground system using matlab and simulation.

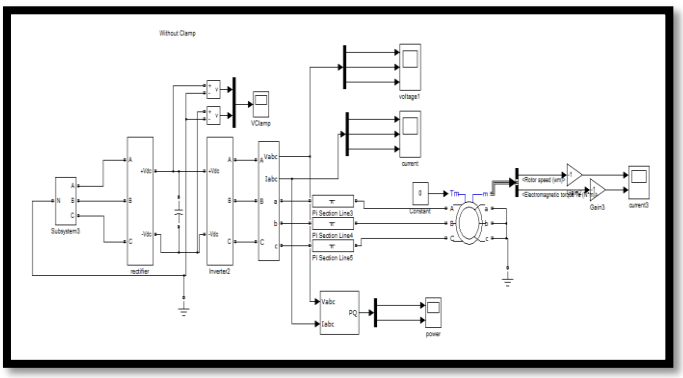

Fig 3a. *Proposed without clamp ciricuit is for solid Y ground system using matlab and simulation*

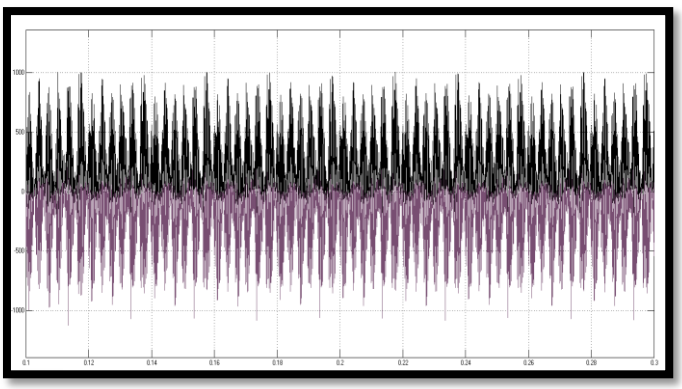

Fig.3b *Simulation result of without clamp with Y grounded system*

From equation 4.

$$Vpg = Vpgpk\_DM + Vcmpk = \left(2.5 - \frac{4Cf}{Ccmo+2Cf}\right)Vdc$$

Vpg = Vpgpk_DM – Vcmpk = - $\left(2.5 - \frac{4Cf}{Ccmo+2Cf} \right)$Vdc

Vpg = Vpgpk_DM + Vcmpk = (2.5 – 0) 618
= 1545V.

Vng = Vngpk_DM + Vcmpk = - (2.5 – 0)618
= -1545V.

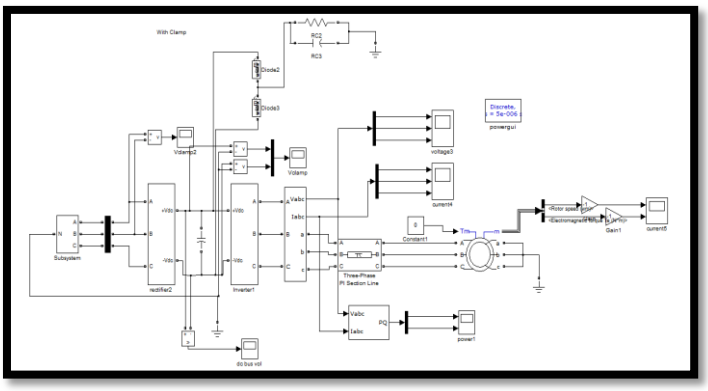

Fig 4a. *Proposed with clamp ciricuit for a solid Y ground system using matlab and simulation*

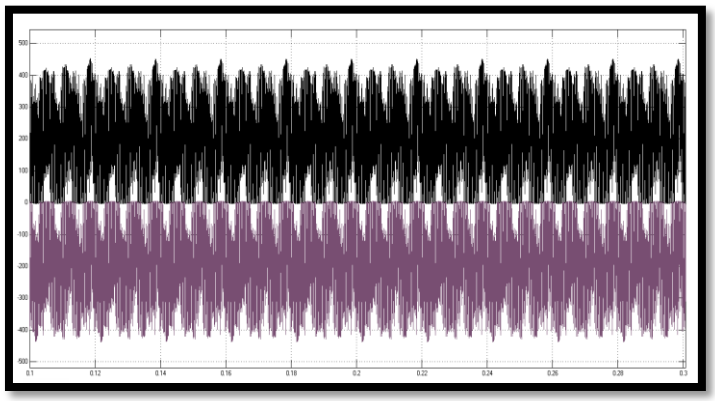

Fig.4b *simulation result of with clamp circuit with Y grounded system.*

To verify the highest voltage stress between bus terminals and the GND. Common mode capacitance is manually reduced to 0.001 uF. The output speed of the inverter is set at 0 Hz during simulation.

Fig. 4a and fig 4b shows the voltage between GND and dc+ with and without the clamp circuit under Y grounded system. The dc bus voltage of the inverter is simulated as 618 V. From this figure, it can be found that the voltage stress between dc bus terminals to GND may increase to as high as 1528 V without the clamp circuit around 2.47 times of the dc bus voltage. The high voltage stress as estimated in Section II is clearly verified. With the clamp circuit, the voltage drops to around 618 V as shown in Fig. 6. The voltage stresses reduces 910 V with the clamp circuit added

2. Proposed without and with clamp ciricuit for a solid corner ground system using matlab and simulation

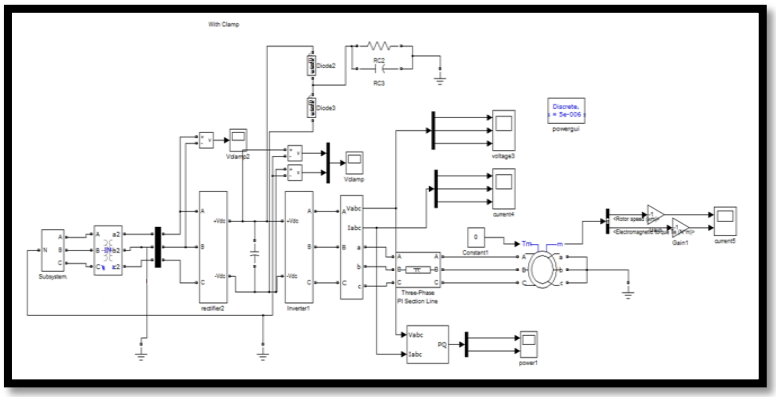

Fig. 5a *Proposed without clamp ciricuit for a solid corner ground system using matlab and simulation*

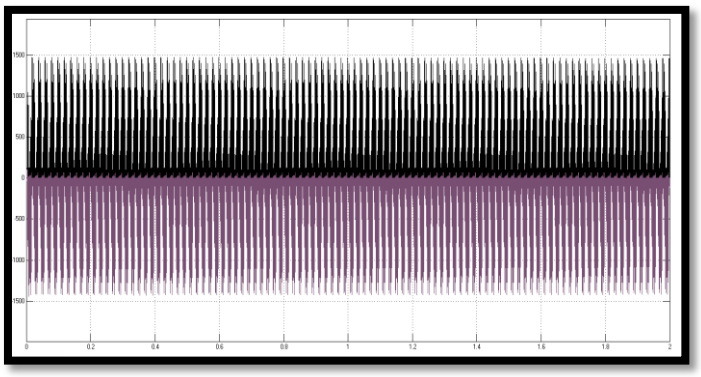

Fig.5b *Simulation result of without clamp with corner grounded system*

From equation 5

Vpg = Vpgpk_DM + Vcmpk = (3 - $\frac{4Cf}{Ccmo+2Cf}$)Vdc

Vng = Vpgpk_DM - Vcmpk = - (3 - $\frac{4Cf}{Ccmo+2Cf}$)Vdc

Vpg = Vpgpk_DM + Vcmpk = (3 – 0) 694

= 2081V.

Vng = Vngpk_DM + vcmpk = - (3 – 0) 694

= -2081V.

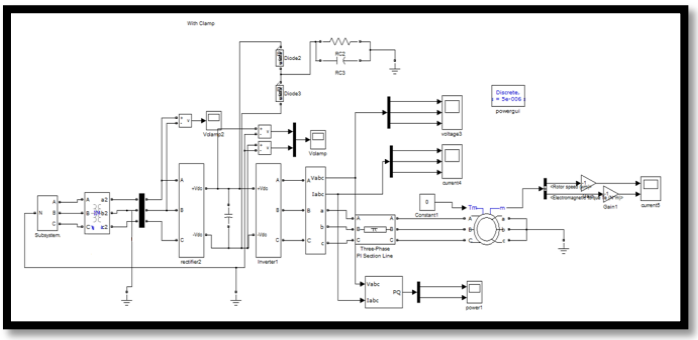

Fig.6a *Proposed with clamp ciricuit fo a solid corner ground system using matlab and simulation*

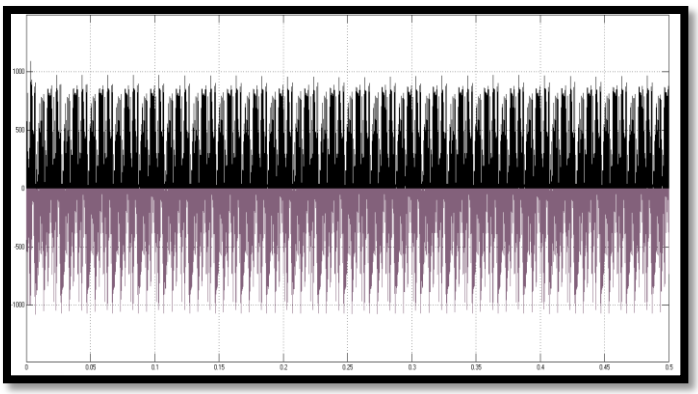

Fig.6b *Simulation result of with clamp with corner grounded system.*

Fig. 6a and 6b further shows the voltage between GND and dc+ with and without the clamp circuit under corner grounded system (input phase B is grounded). The dc bus voltage of the inverter is simulated as 691 V. From this figure, it can be found that the voltage stress between dc bus terminals to GND may increase to as high as 2081 V without the clamp circuit-around 3 time of the dc bus voltage. The high voltage stress as estimated in Section II is clearly verified. With the clamp circuit, the voltage drops to around 710 V as shown in Fig. 6b. The voltage stresses reduces 1371 V with the clamp circuit added. For both conditions, the effectiveness of clamp circuit is clearly verified. It helps to clamp the bus terminals to GND to slightly higher than the dc bus voltage.

3. To Prevent Voltage Stresses While Rectifier is Anti-Biased:

Under this condition, the system is High Resistance Grounded (HRG) at the source neutral with a grounding resistor of 300 Ω. The common mode capacitance of the drive is set as the same capacitance (0.1 uF) as in the drive.

Proposed without and with clamp ciricuit for Prevent Voltage Stresses While Rectifier is Anti-Biased:

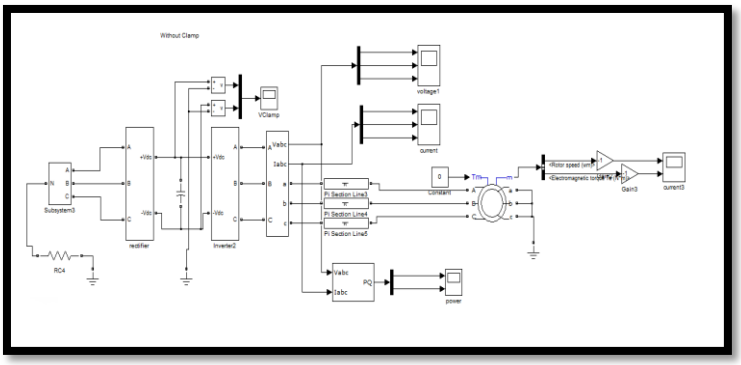

Fig 7a. *Proposed without clamp ciricuit for Prevent Voltage Stresses While Rectifier is Anti-Biased*

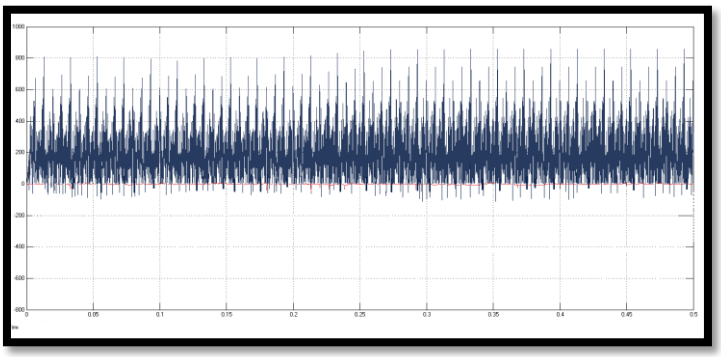

Fig.7b *Simulation result of without clamp with Rectifier is Anti-Biased.*

Fig. 7a and 7b shows the voltage between GND and dc+ with and without the clamp circuit for the single drive case during drive deceleration. The waveforms are taken at about drive output frequency of about 0 Hz and also the SCRs at the lower legs of the rectifier being turned off. It can be seen that this voltage may increase to as high as 1138 V without the clamp circuit.

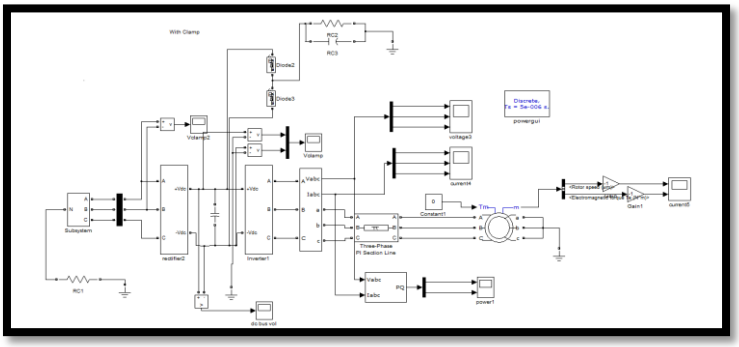

Fig 8a. *Proposed with clamp ciricuit for Prevent Voltage Stresses While Rectifier is Anti-Biased.*

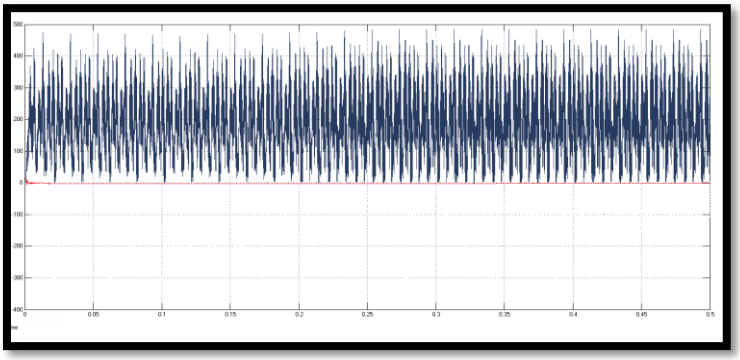

Fig.8b *Simulation result of with clamp with Rectifier is Anti-Biased.*

Fig. 8a and fig 8b with the clamp circuit, the voltage drops to 669V. The voltage stress reduces 469 V by the clamp circuit.

Summary:

For all above cases, the voltage stresses between dc bus terminals to the GND are much higher than the dc bus voltage without the clamp circuit. After the clamp circuit is added, the voltages are slightly higher than dc bus voltage. The effectiveness of the circuit is clearly verified.

5. CONCLUSION

This paper investigated the effect of PWM switching into long motor cables on the voltage stresses of different components inside an ASD. It was shown that a potential voltage insulation problem may exist on certain ASD components and cause insulation failures under several extreme operating conditions. A dc bus voltage clamp circuit was proposed to mitigate the increased stresses. Simulation and experimental result were provided to verify its effectiveness. With the proposed clamp circuit, the voltage between the GND and dc bus terminals are all clamped to the slightly higher than the value dc bus voltage.

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