A Low-Power High-speed Pipelined Accumulator Design Using CMOS Logic for DSP Applications

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Abstract: *The pipelined accumulator forms the basic building block of arithmetic modules for DSP applications. The basic building block of an accumulator unit is the adder cell and data storage registers e.g. Flip-Flop (FF). The operational speed of FF determines the correctness and accuracy of the functionality of 12BDA. The high-speed full adders that use low power consumption is a fundamental arithmetic operation that can never be neglected in accumulator unit, and it is one of the speed-limiting elements. The efficiency of the accumulator unit is determined by the adder cell taken in to account.In this paper, a 12-Bit pipelined accumulator cell optimized for low power and high speed operation are proposed. Update rates of 150MHz are achieved by careful choice of architecture. The static, D-type flip flops used in the pipeline architecture are the dominant source of power dissipation. Hence the refresh-every-cycle operation of accumulators is exploited by using dynamic delay elements to reduce power consumption The accumulator unit is simulated with mentor graphics using the 130nm CMOS technology at different supply voltages ranges. Various metrics such as delay, static and dynamic power are simulated and reported for both pipelined and non-pipelined accumulator unit for different adder topologies.*

Keywords: *Accumulator, Low-power, VLSI, Pipelining*

1. INTRODUCTION

Low power applications have become one of the main concern for VLSI system designers. With the extensive growth in digital systems, and the evolution of the shrinking technology, the research effort in low-power electronics for reducing circuit delay, power consumption, area and threshold voltage in response to the increasing in the number of transistors has been intensified. Energy-efficiency is other important criteria needed for all VLSI systems that demand the need of low-power functional units that enable the implementation of long-lasting battery-operated systems with high throughput and operating frequency. The semiconductor industry has marked a tremendous growth in multimedia-based applications. Fast arithmetic computation cells including adders and multipliers are the most frequently and widely used circuits in very-large-scale integration (VLSI) systems. One of such arithmetic unit is the accumulator unit that is used in various DSP applications.

The basic building block of an accumulator unit is the adder cell and data storage registers e.g. Flip-Flop (FF). The operational speed of FF determines the correctness and accuracy of the functionality of 12BDA. The high-speed full adders that use low power consumption is a fundamental arithmetic operation that can never be neglected in accumulator unit, and it is one of the speed-limiting elements. The efficiency of the accumulator unit is determined by the adder cell taken in to account. We need a faster respond adder. Hence optimization of the adder both in terms of speed and power consumption should be considered.

The review is organized section wise. Section 2 highlights the conventional static and dynamic full adder modules used for comparison. In Section 3 explains the design and implementation of 12 bit pipelined accumulator unit for DSP application. Section 4 describes the simulation result. Section 5 concludes the result.

2. REVIEW OF FULL ADDERS

2.1. Static Full Adder Cells

The conventional CMOS adder cell (fig.1) using 28 transistors has high power consumption due to high number of transistors [2]. The PT adder cell (fig.2) has threshold drop, so that the signals have to be amplified by using CMOS inverters at the outputs. Also they consume less power [3].The Complementary Pass Transistor Logic (CPL) with swing restoration (fig.3) uses 32 transistors produces many intermediate nodes and their complement to give the outputs [2].Transmission gate full adder cells (fig.4) with 20 transistors have no voltage drop at output node, but it requires twice the number of transistors than PTL to design similar function [2]. The transmission function full adder (fig.5) has two possible short circuits paths to ground. This design uses pull-up and pull-down logic as well as complementary pass Logic to drive the load
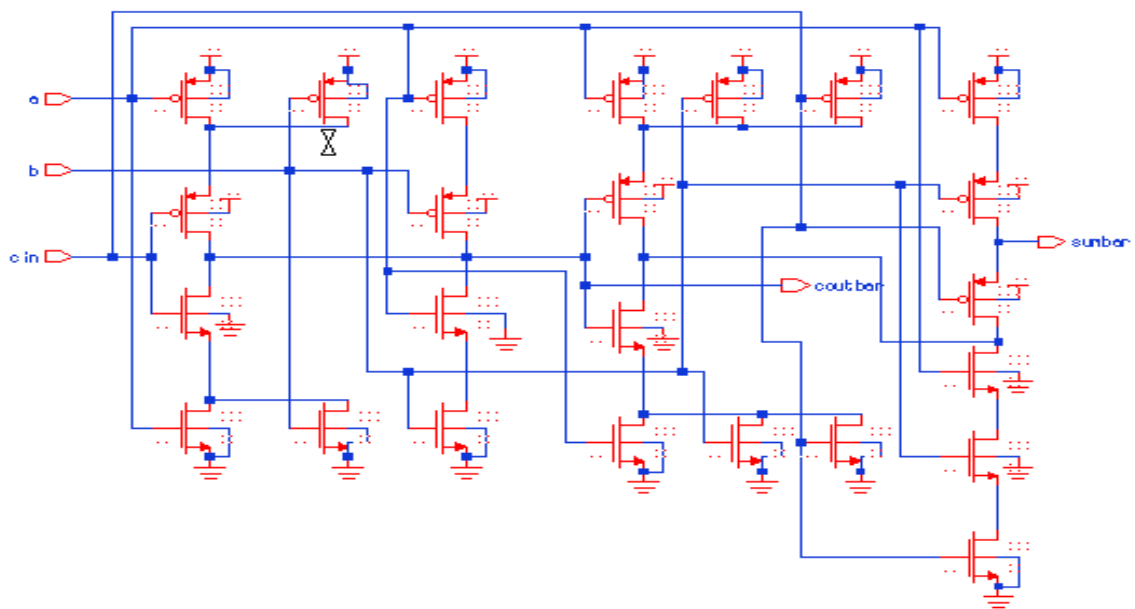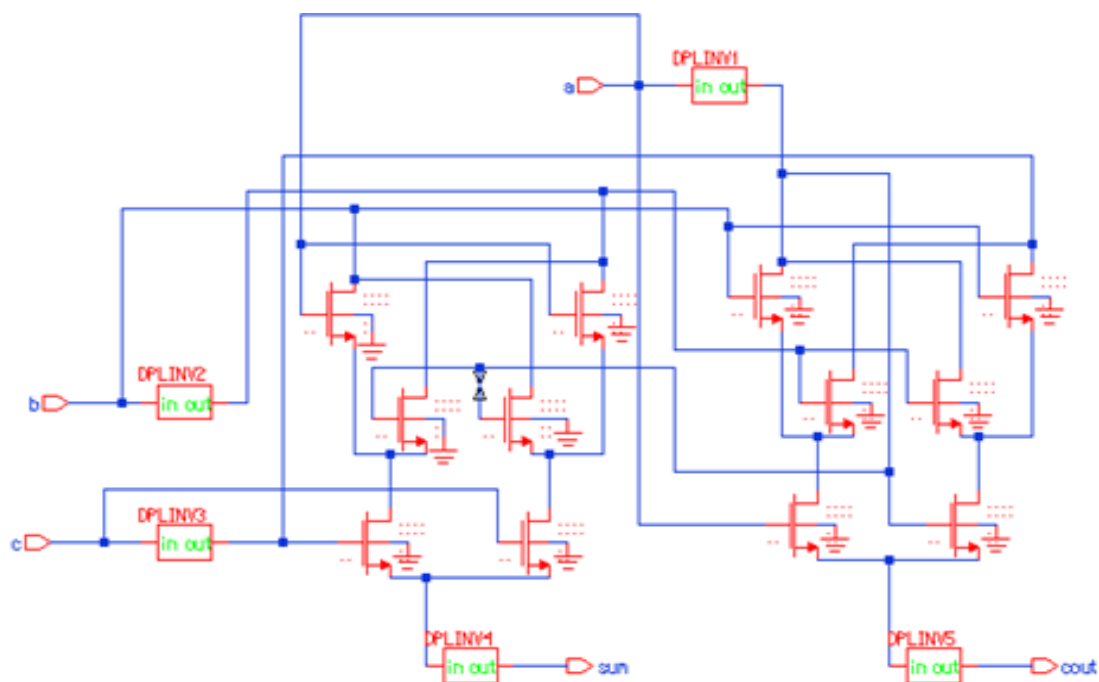

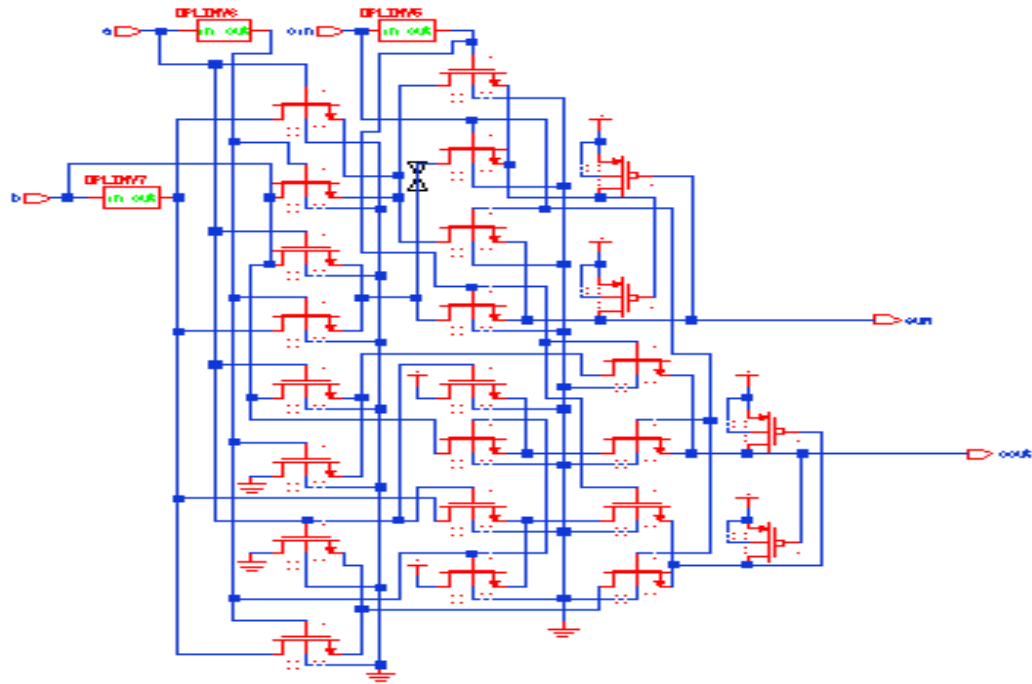**Fig1.** *Conventional CMOS full adder*

Fig2. *PT full adder*
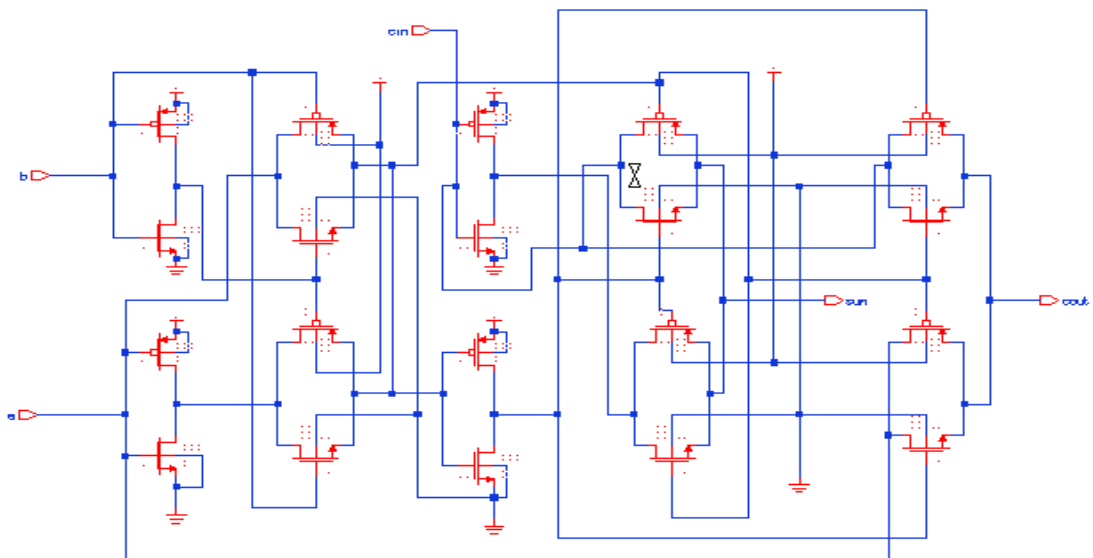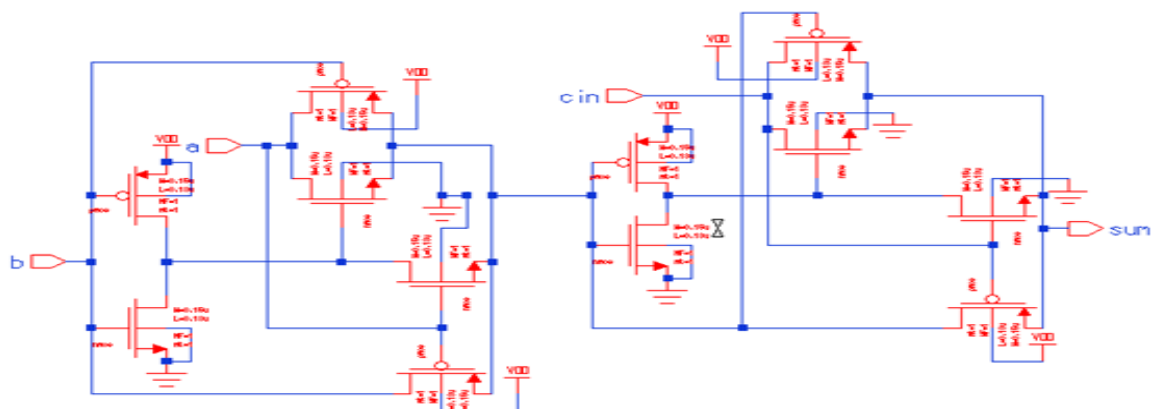
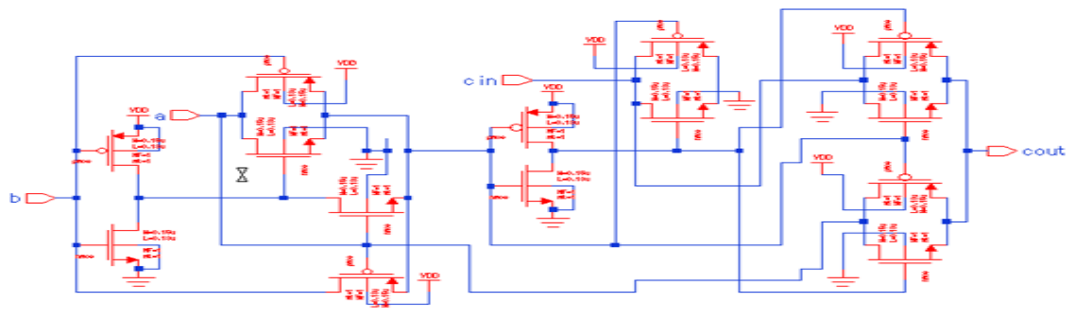**Fig3.** *CPL full adder*

Fig4. *TG full adder*

Fig5. *TF full adder*

Hybrid full adder (fig.6) has been designed with pass logic circuit cogenerates the intermediate XOR - XNOR and hence improves outputs [2]. A new 14T full adder (fig.7) is the low power implementation of the full-adder that can reliably operate within certain bounds when the power supply voltage is scaled down [2].
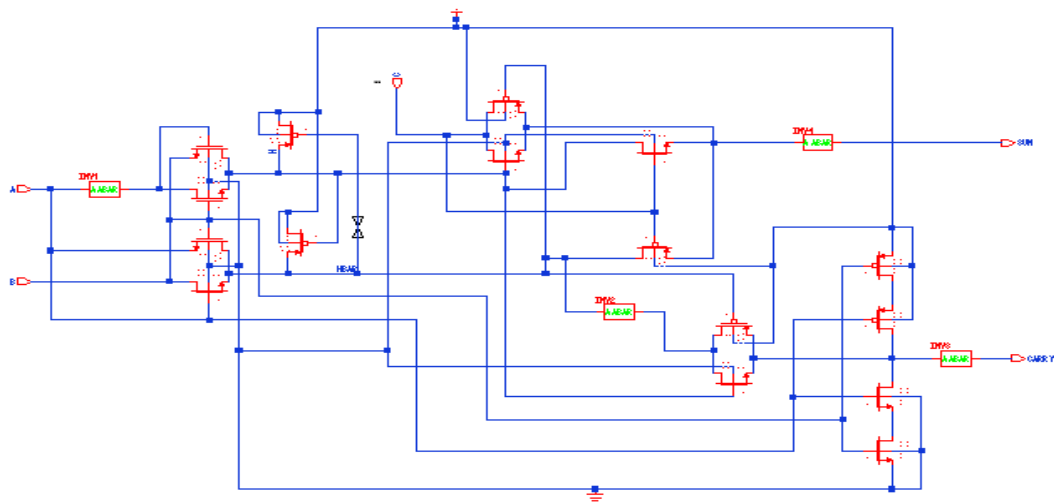

Fig6. *Hybrid full adder*

The new HPSC full adder (fig.8) whose simultaneous generation of XOR and XNOR outputs by pass logic is advantageously exploited to a novel complementary CMOS stage to produce full-swing and balanced outputs so that adder cells can be cascaded without buffer insertion.[10]. For DPL full adder cells (fig.9) and the SR-CPL full-adder (fig.10) there are no signals generated internally that control the selection of the output multiplexers reducing so the overall propagation delays. The capacitive load for the C input has been reduced. [2].
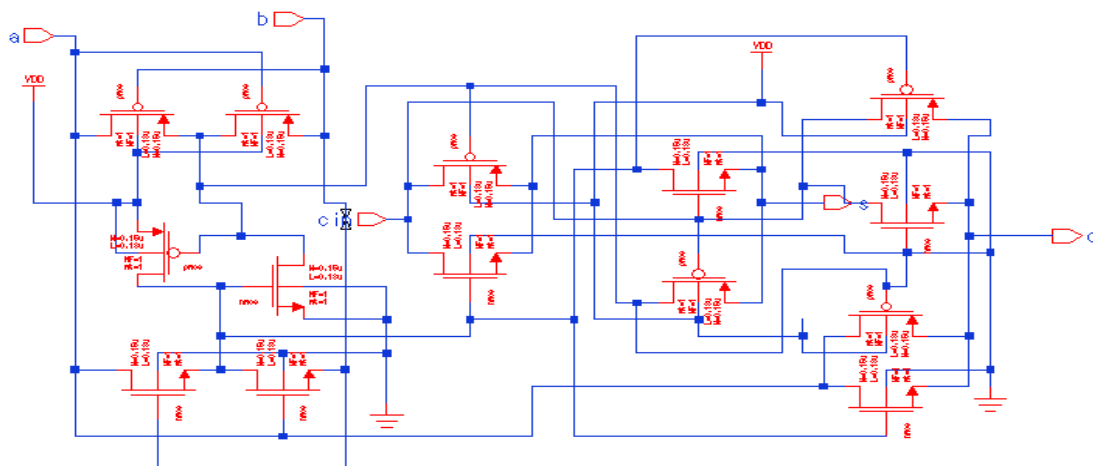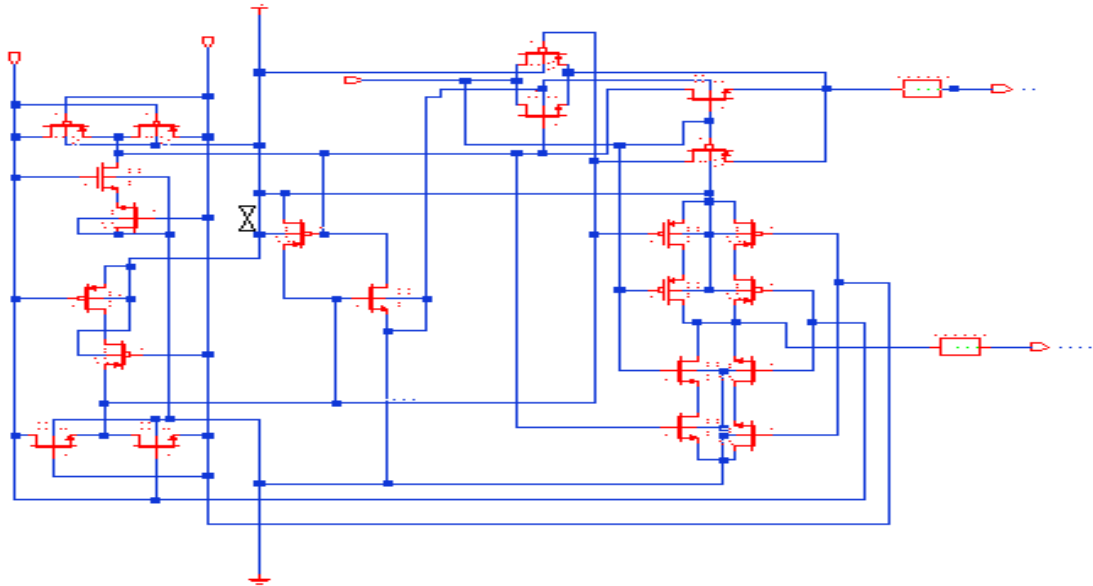

Fig7. *New 14T full adder*

Fig8. *New HPSC full adder*
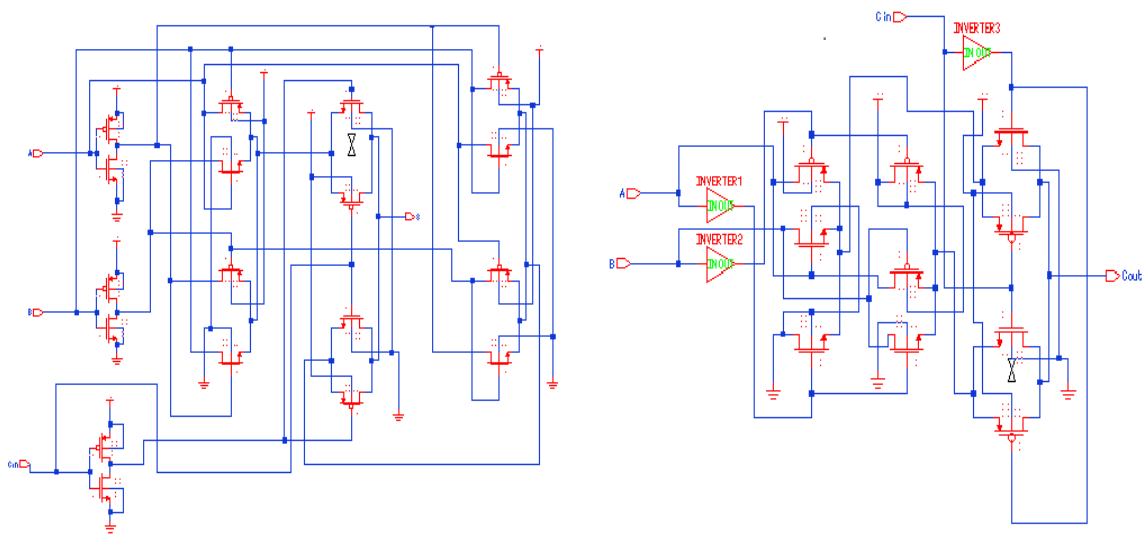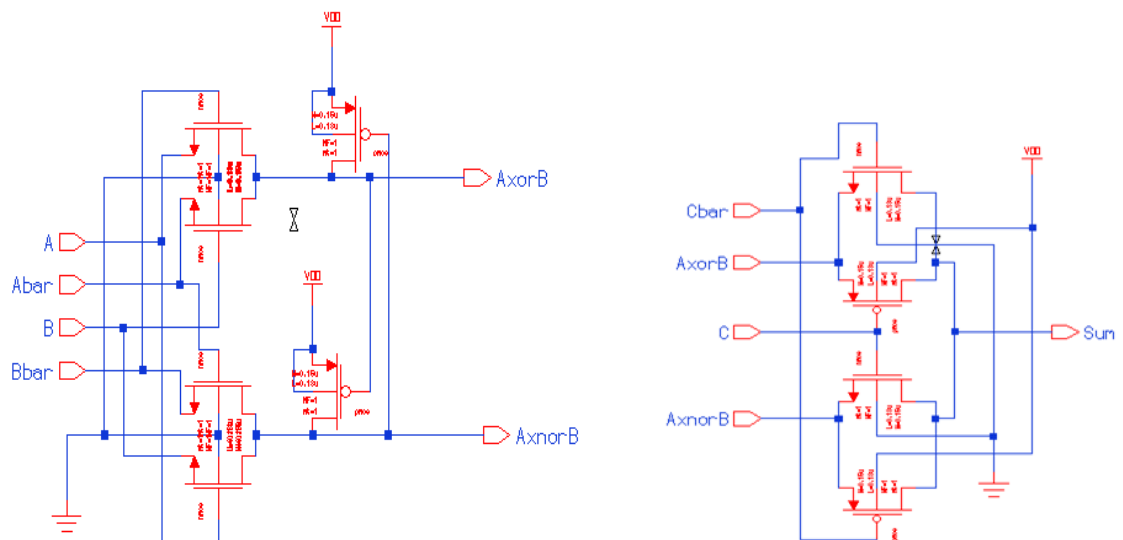

Fig. 9. *DPL Full-adder*

Fig10. *SR-CPL Full-adder*

2.2. Dynamic Full Adder

The dynamic conventional CMOS FA (fig.11), where the additional dynamic latches at the outputs perform the logic inversion, buffering, and pipelining functions [5].
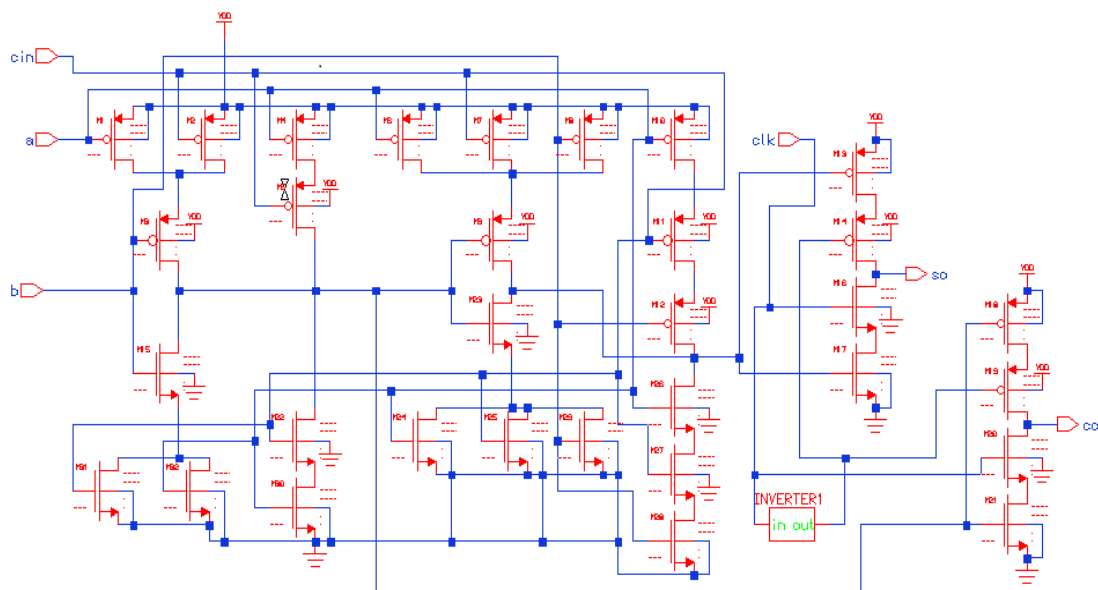

Fig11. *Dynamic conventional CMOS FA*

The pseudo-NMOS pipelined FA cell (fig.12) has latches added at the outputs. The P-logic trees (P-blocks) in its conventional CMOS counterpart have been replaced with pull-up P-MOSFET's which are always weakly on. The NP complementary dynamic CMOS full adder (fig.13) is based on Zipper (NP) technique. It has full swing voltage levels. Clock and Clock' signals cause both stages of the circuit to enter the evaluation phase simultaneously [5].The PN complementary dynamic CMOS full adder (fig.14) is implemented in two level dynamic CMOS logic style with PN technique. The standard N-P domino FA cell (fig.15) is a variation of a NORA-CMOS serial full adder [5]. The quasi N-P domino FA cell (Fig. 16) results in a higher speed but also requires the use of latches. The N-block that computes the sum (So) output has a behaviour similar to that of P-block except that the directions of precharging and evaluation on node 2 are both opposite to those on node 1.
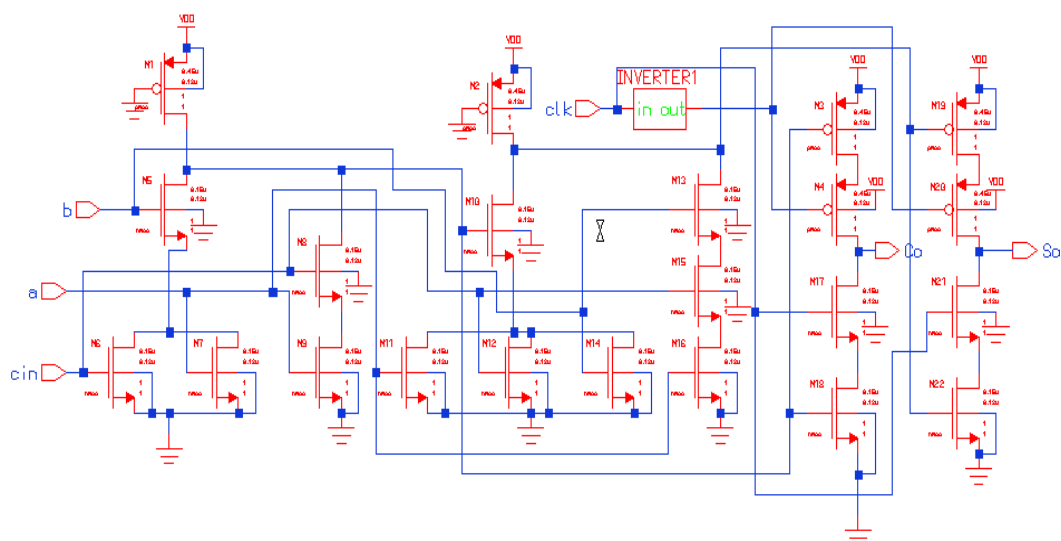

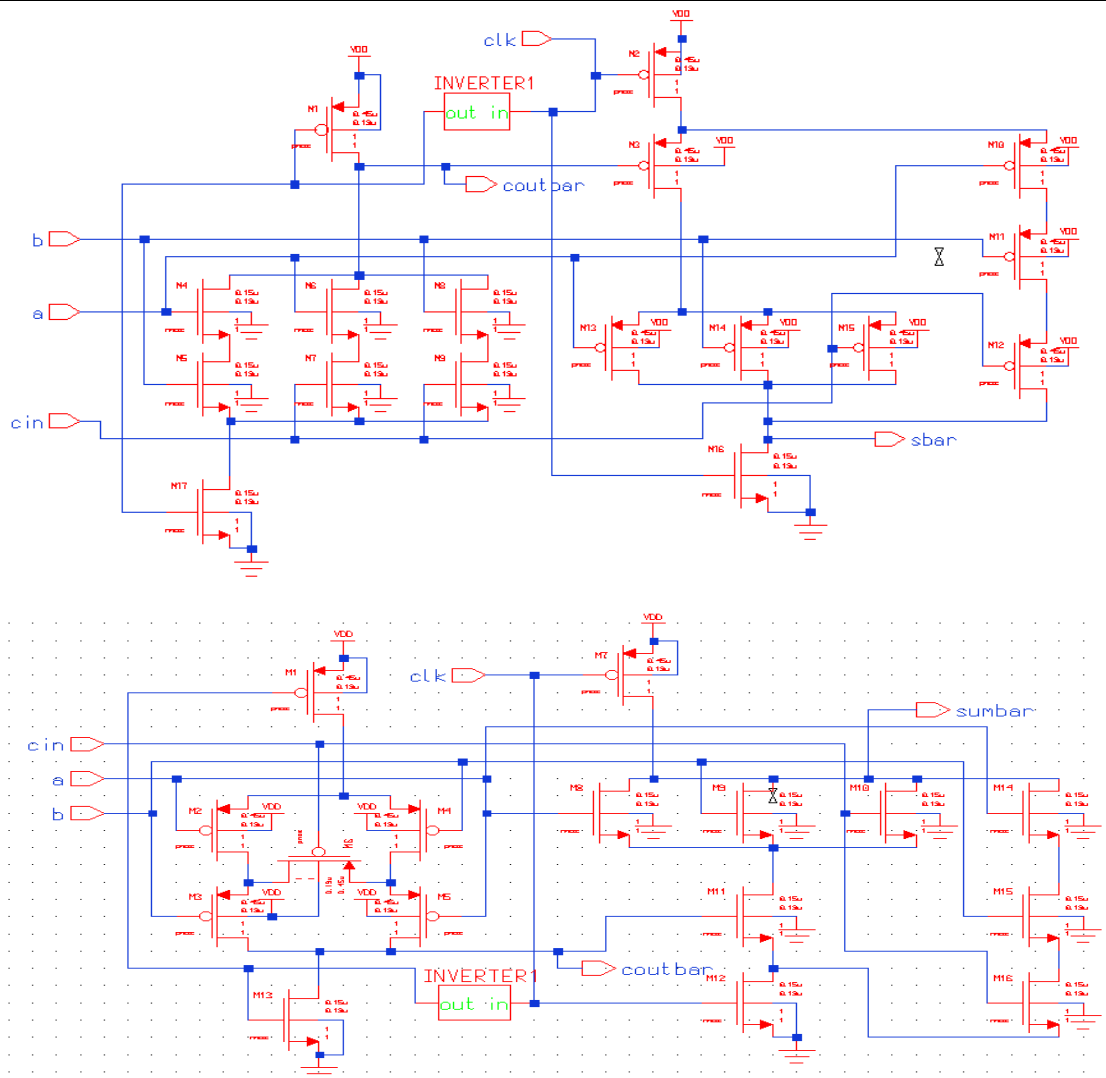**Fig12.** *Pseudo-NMOS pipelined FA cell*

Fig13. *NP-CMOS Full Adder*

Fig14. *PN complementary dynamic CMOS full adder*
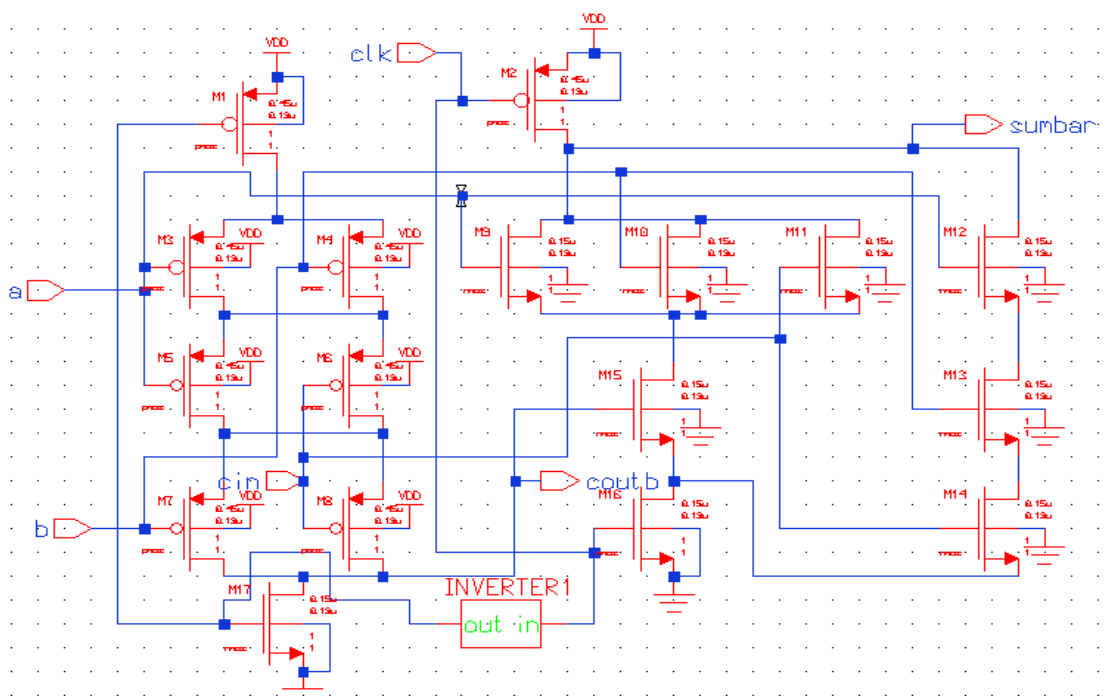
The Multi Output dynamic logic (fig.17) uses one Clock signal, but the speed of this circuit is reduced due to the PMOS transistors used in its design. The other disadvantage of this implementation is that this circuit is not Full Swing, Another model in (fig.18) eliminates charge sharing problem.
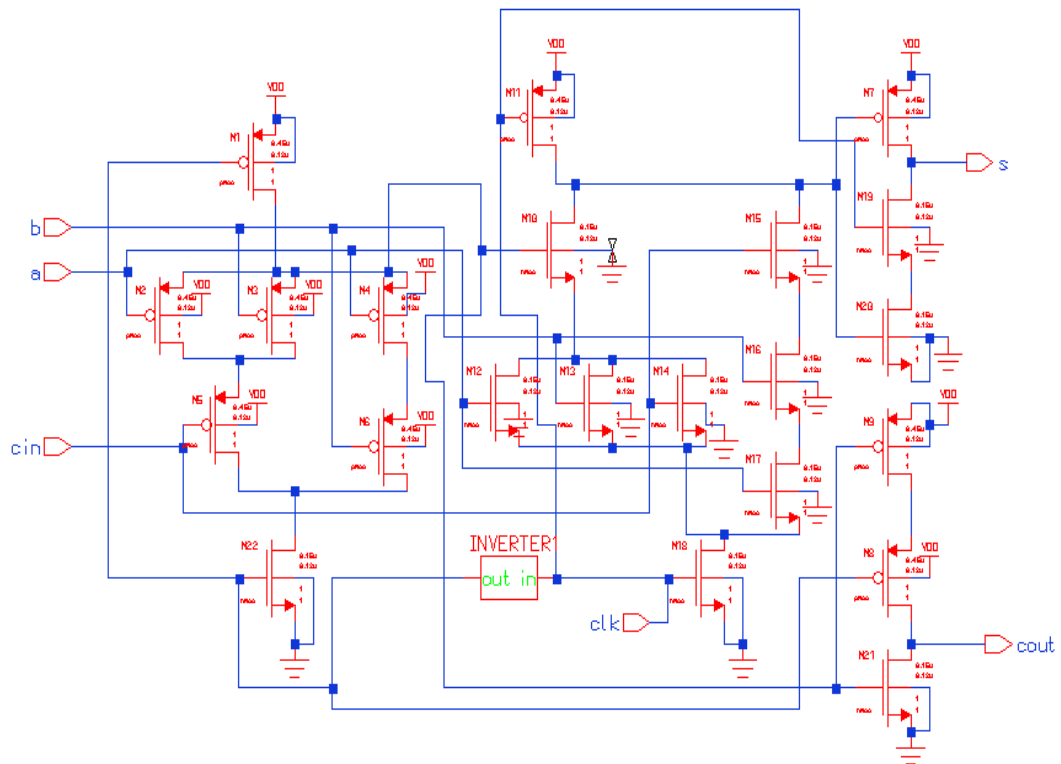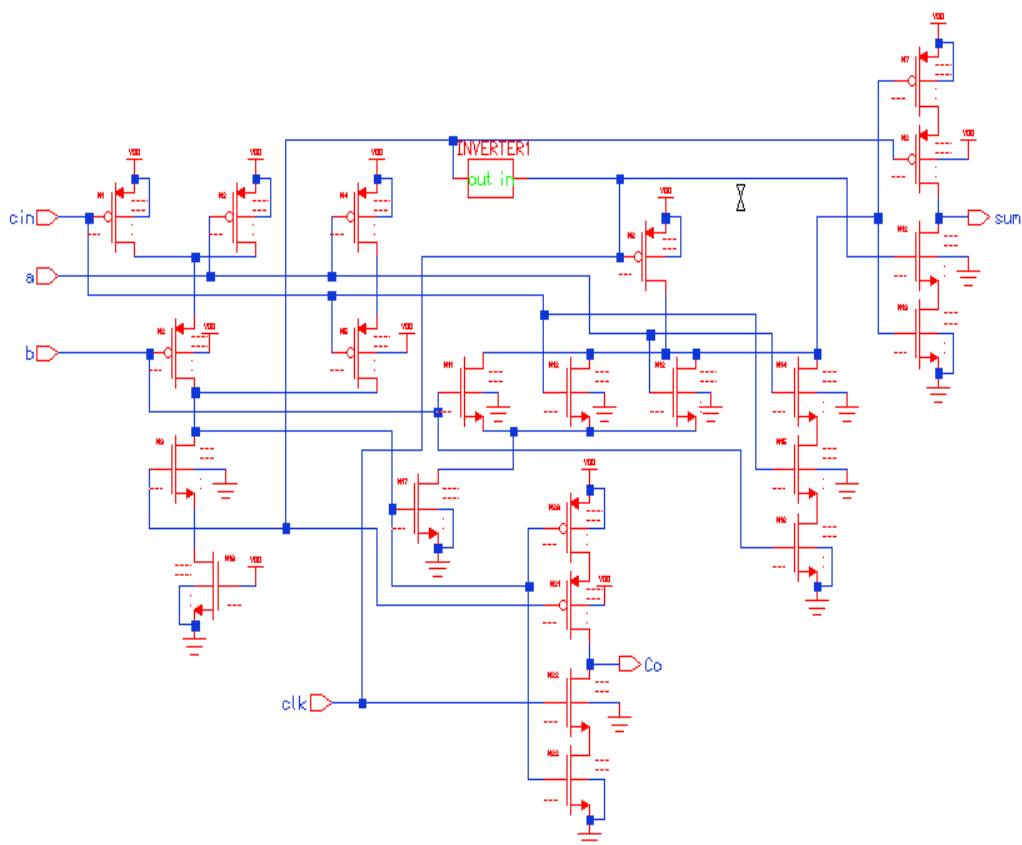

Fig15. *N-P domino FA cell*

Fig16. *quasi N-P domino FA cell*
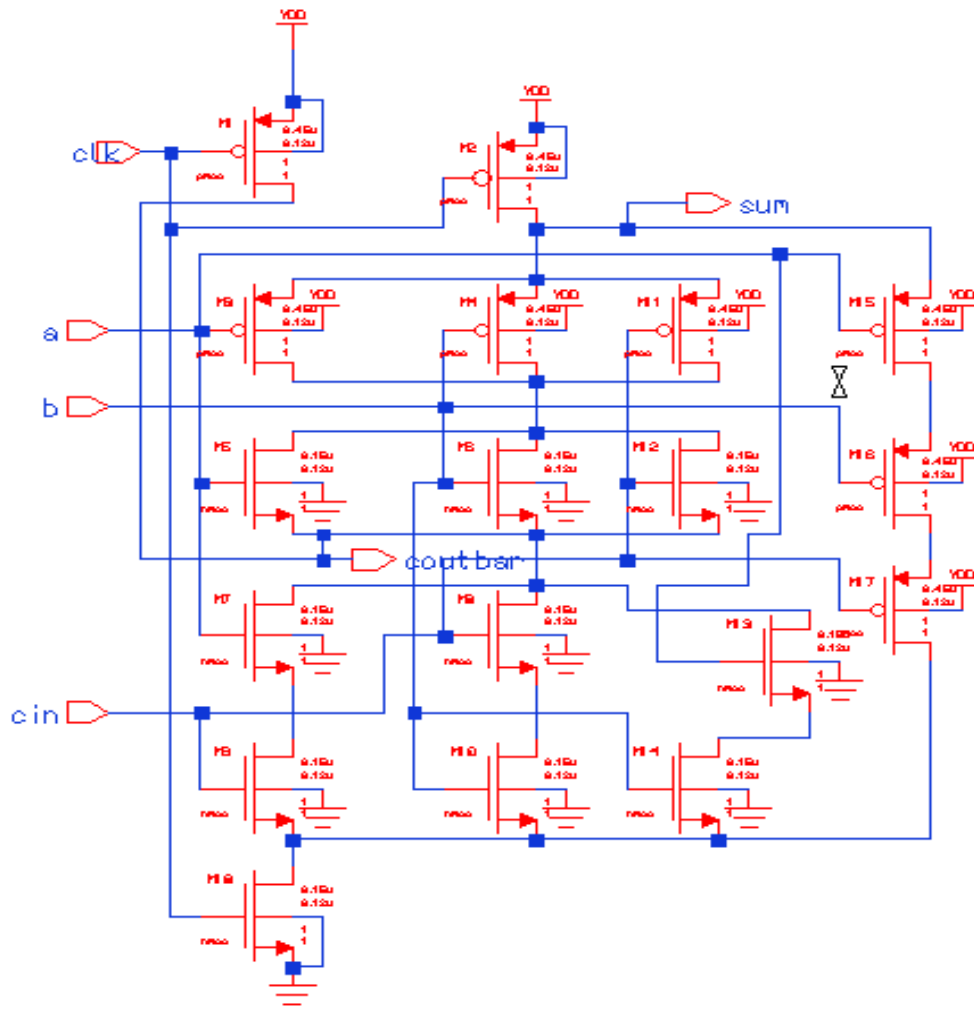
Fig17. *Multi Output dynamic logic*
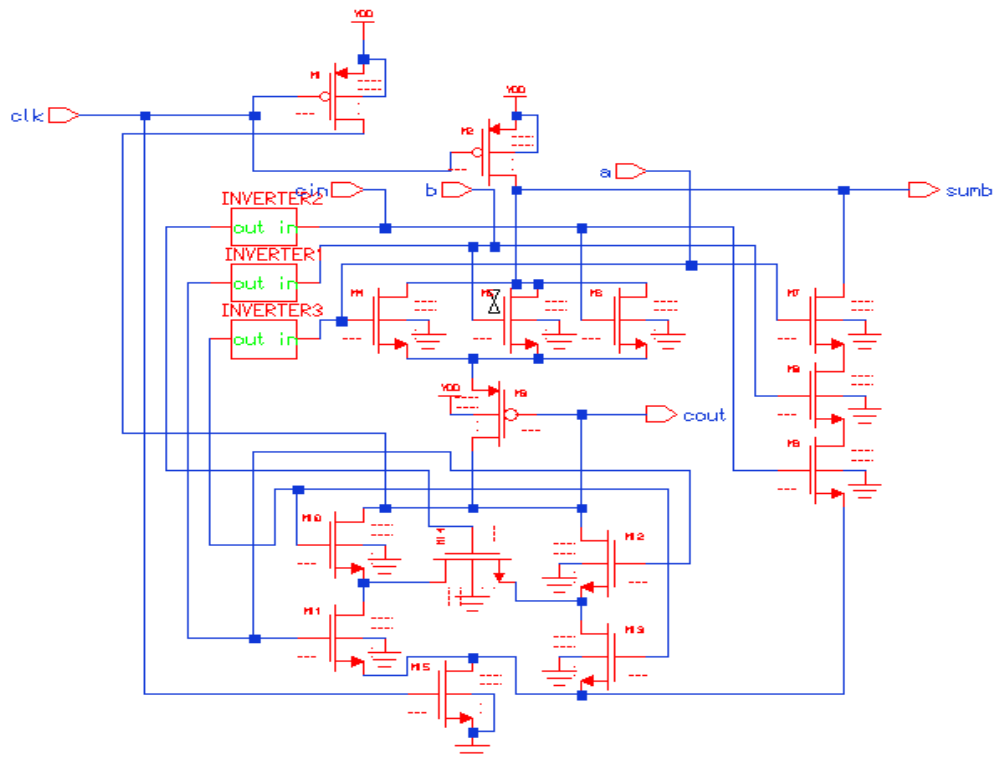
Fig18. *Multi Output Dynamic Logic*

3. 12-BIT PIPELINED ACCUMULATOR STRUCTURE

The general block diagram of 1-bit accumulator cell is shown in fig.19.
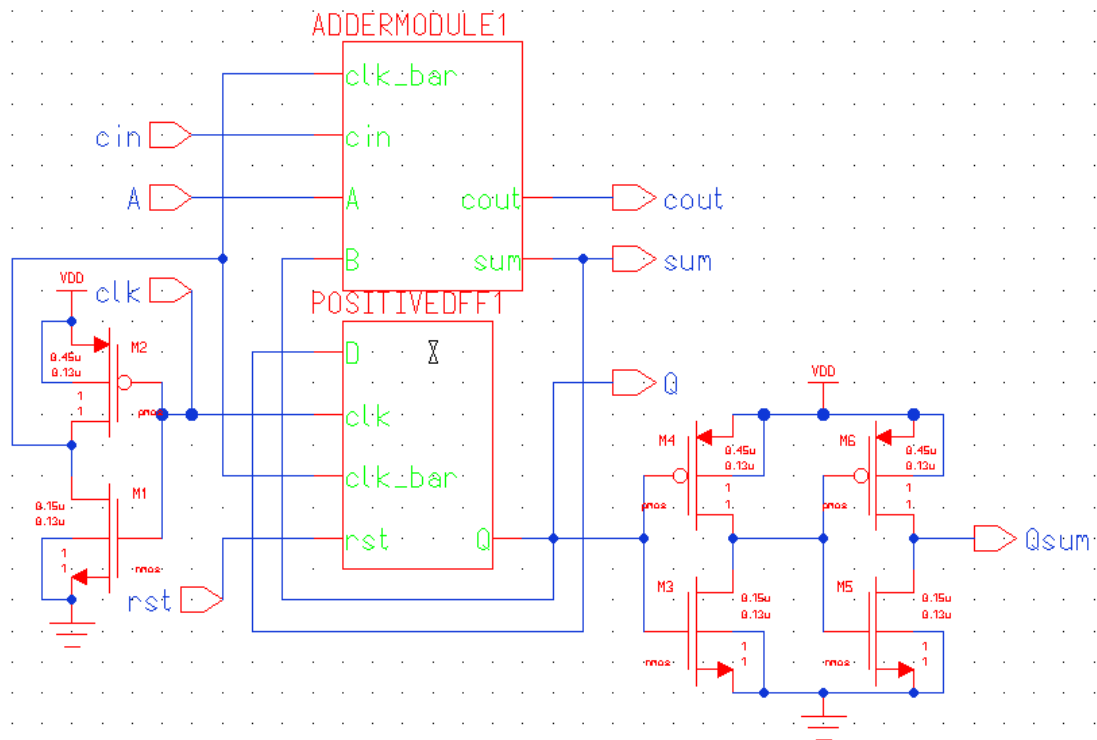
Fig19. *Block diagram of 1-bit accumulator cell*

3.1. Pipelining

Pipeline is to divide a big stage in smaller independent combinatorial sub-stages (or sub-tasks), that works at the same time on a part of the throughput [1]. In every sub-stage, a register stores the result of the previous sub-stage and feeds it to the following stage at the following clock pulse. The maximum update rate of a pipelined accumulator is limited by the time it takes for the carry to propagate through the adder in the system.

3.2. 12 Bit Pipelined Accumulator

By partitioning the carry propagation path with latches a pipelined accumulator (fig.20) is obtained [1].
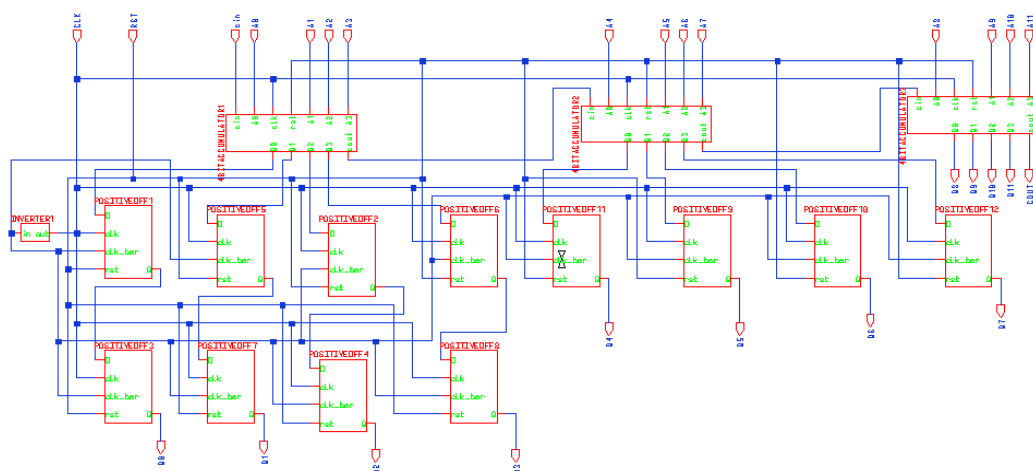
Fig20. *12-Bit pipelined accumulator*

Since pipelining is implemented in design, accumulator can work up to a clock frequency of 150 MHz . Designing of 12 bit accumulator is carried out by pipelining three 4 bit accumulators.

4. SIMULATION RESULTS

Several static full adders were compared in terms of propagation delay, power dissipation and area(Table 1). The output of12-bit pipelined accumulator is shown in fig. 21.

Fig21. *12-bit pipelined accumulator*

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Table1. *Comparisons o f Power, Delay and Area of Static and Dynamic Adder Cells*

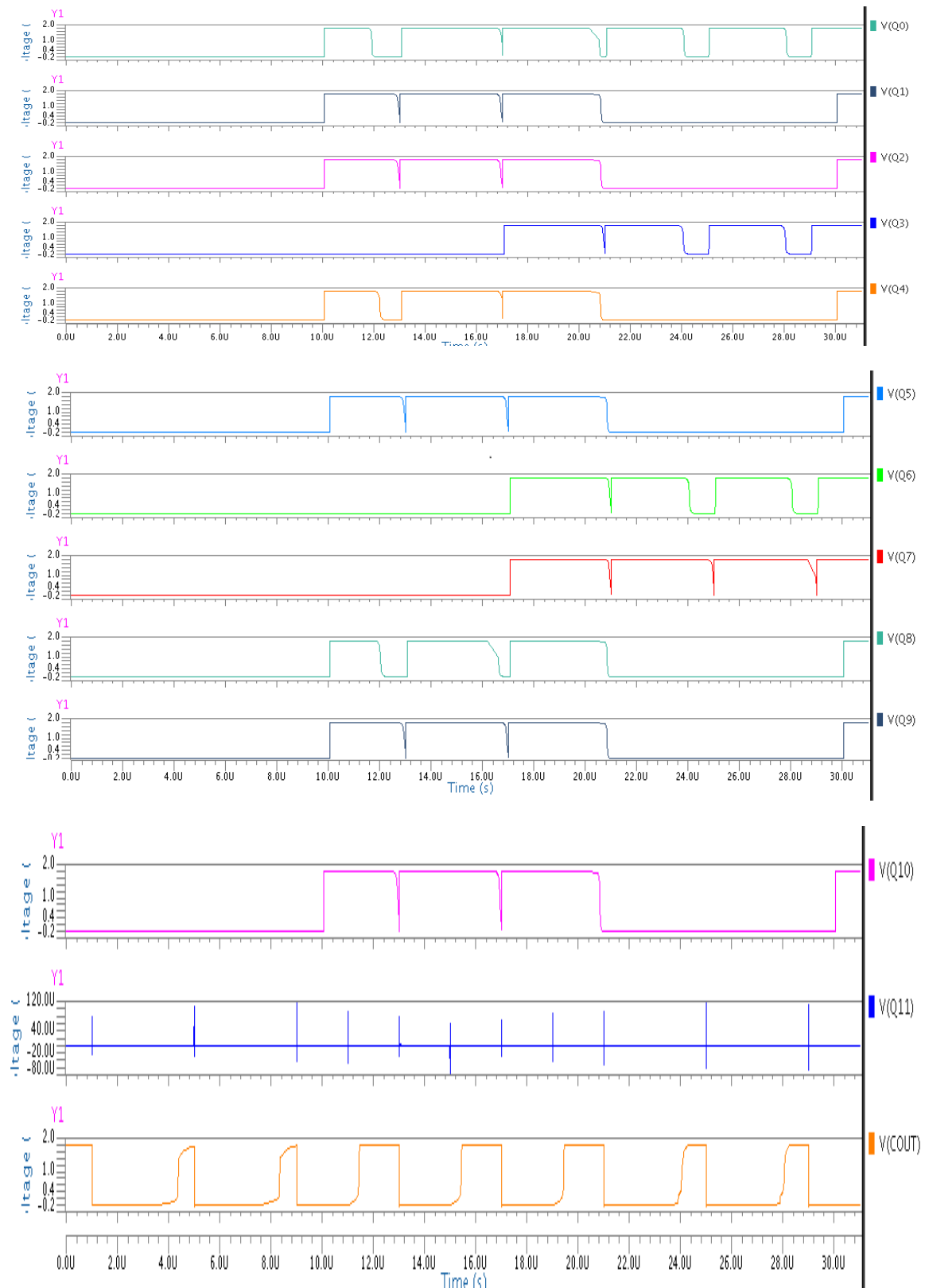| SL. NO.	NAME OF FULL ADDER ELL	STATIC POWER DISSIPATION(NW)			DYNAMIC POWER DISSIPATION (NW)	DELAY (PS)	AREA (NO.OF TRANSI STORS)
		1.8V	3.3V	5V			
STATIC FULL ADDERS							
1	C-CMOS	129.54	567.34	1267.127	252.60	524.1	28
2	PTL	67.6116	185	476.77	23.96	498.58	16
3	CPL	103.56	564.76	1635.725	1.24uW	389.96	32
4	TG	99.383	224.12	582.34	21.06	333.32	20
5	TF	67.415	190.45	456.98	13.24	299.56	16
6	HYBRID	1206.5	1.2uW	11.34uW	468.85	241.90	26
7	HPSC	52.33	78.50	130.93	12.17	219.20	22
8	NEW HPSC	55.49	75.77	125.78	273.78	210.11	26
9	NEW 14T	115.113	302.56	852.33	273.78	406.54	14
10	DPL	44.986	64.25	110.32	41.82	205.22	28
11	SR-CPL	44.88	65.21	105.22	33.27	187.63	26
DYNAMIC FULL ADDERS							
12	C- CMOS	16.31	27.76	72.65	23.51	193.60	32
13	PSEUDO-NMOS	11.21	34.05	86.59	23.52	303.48	22
14	NP-CMOS	6.13	21.55	59.55	6.41	209.20	17
15	PN-CMOS	4.74	14.48	36.98	6.96	260.50	16
16	DUAL-RAIL	24.30	44.32	108.09	540.48	291.06	40
17	NP-DOMINO	4.74	14.48	23.25	7.36	254.16	22
18	PN-DOMINO	4.74	14.49	36.98	6.58	271.81	17
19	ZIPPER	6.12	20.09	52.33	11.07	292.11	16
20	MULTIOUTPUT1	4.16	13.67	35.70	5.48	341.71	18
21	MULTIOUTPUT2	9.67	34.56	95.71	21.08	1.01nS	14
22	QUASI –NP	463.54	3.02uw	4.99uW	238.09uW	126.53	23

5. CONCLUSION

An accumulator has been designed based upon a pipelined architecture, tailored to have a 12 bit input and a 13 bit output that operates at 150 MHz .The accumulator cell has a power consumption of 1.96mw and delay of 126.53 ps. Power savings have been obtained by the use of a delay element, suitable for accumulators within a DSP system, rather than from a standard cell library. Attempts to reduce power consumption and propagation delay were carried out further by using efficient optimization of adder cell within the accumulator

REFERENCES

[1] Fang Lu, Member, IEEE, and Henry Samueli, Member, IEEE "A 200-mhz CMOS pipelinedmultiplier-Accumulator Using a Quasi-dominodynamic Full- Adder Cell Design" IEEE journal of solid-state circuits, vol. 28, no. 2, february 1993.

[2] Massimo Alioto, Member, IEEE, and Gaetano Palumbo, Senior Member, IEEE "Analysis and Comparison on Full Adder Block in Submicron Technology"IEEE transactions on very large scale integration (vlsi) systems, vol. 10, no. 6, december 2002.

[3] Kanika Kaur and Arti Noor "power estimation analysis for cmos cell structures ", International Journal of Advances in Engineering & Technology IJAET ISSN: 2231-1963 293 Vol. 3, Issue 2, pp. 293-301 May 2012.

[4] Reza Faghih Mirzaee, Mohammad Hossein Moaiyeri, Keivan Navi"High Speed NP-CMOS and Multi-Output Dynamic Full Adder Cells" International Journal of Electrical and ElectronicsEngineering4:42010.

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Tresa Joseph (Assistant Professor) received B.Tech degree in Electronics and communication engineering from Calicut University in 2011and M.Tech degree in VLSI and Embedded Systems from Mahatma Gandhi University in 2013. She is currently Assistant Professor in sahrdaya College of Engineering and Technology, Kerala. Her research interest includes VLSI Design of semi or full custom chips for implementation of specific architecture and Low power VLSI Design.