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Design and Power Analysis of 8T SRAM Cell Using Charge Sharing Technique

Lingam Rajesh

M.TECH Mallareaddy Eng College (VLSISD) Hyderabad
ls.rajeshece@gmail.com

Santosh J

Assistant Professor in ECE at MREC, Hyderabad

Abstract: *The aim of the paper is to design and analyze 8T SRAM Cell using Charge Sharing Technique where a standard 8T SRAM cell performance degrades with low power supplies. In the design the SRAM cell uses a charge sharing technique between the transistors to make SRAM more rigid against noises that occur due to low power supplies. Apart from noise reduction the read discharge power is reused. The comparison between standard 6T, 8T and 8T with charge sharing is made. It shows that less power is consumed by 8T with charge sharing than others.*

Keywords: *6T SRAM, 8T SRAM, CMOS, dynamic power budge, SNM*

1. INTRODUCTION

Due to growing demand of portable battery operated embedded systems made a necessity for energy efficient design. As predicted 90 % of systems will be made up of memory and the memory management is need of the time. The SRAM is popular choice for embedded systems for its high speed, robustness and ability easy to manufacture. The larger SRAM cell the larger the power consumed.

A basic low power SRAM cell is designed by using cross-coupled CMOS inverters with 6 transistors giving basic 6T SRAM cell. However with technology scaling below nanometer the power dissipation of 6T SRAM becomes significant with low power supplies as due to this the gate delay is increased which reduces the frequency of operations.

An 8T SRAM cell with charge sharing technique which used at architecture level is implemented at the cell level of design.

2. EXISTING WORKS

2.1. Basic SRAM

A number of SRAM cell topologies are reportable within the past years. Among these many design architectures, resistive load four-transistor (4T) SRAM bit cell, that load less 4T cell and 6 transistor(6T) SRAM cell have received attention in use, attributable to their symmetry in storing logic `one' and logic `zero'. The information storage within the 4T SRAM cells is ensured by the leakage current of the access NMOS transistors. Hence, they're not correct candidates for low-power applications. On the opposite hand, the information stability during a 6T SRAM cell is free lance of the outflow current. Moreover, 6T configuration exhibits a significantly higher tolerance against noise that is a very important benefit particularly within the scaled technologies wherever the noise margins area unit lowering. That's the most reason for the recognition of the 6T SRAM cell in low-power SRAM units rather than the 4T configurations in usage.

The Six Transistor SRAM cell is most generally utilized in embedded memory attributable to its quick time interval and relatively little space. 6T cell style involves complex tradeoffs between varied factors specifically abrupt scaling done on area, most sensible soft error immunity ability, high cell on current, low leakage current through off transistors, has good stability with minimum voltage &

minimum word line voltage pulse. The total CMOS 6T SRAM bit cell configuration is shown in Fig.1. Full CMOS SRAM configuration provides greater noise margin, low static or leakage power dissipation, high change speeds suitability for high density SRAM arrays. Every 6T cell contains a capability of storing one little bit of information.

The 6T SRAM cell consists of two inverters connected back to back. M5, M6 are access transistors that are controlled by the word line (WL) pulse. The cell preserves one in all its 2 possible states denoted as 0 and 1 as long as power is obtainable to the 6T bit cell.

There are 3 operations in SRAM memory cell particularly write, browse and storage operations. Read and write operations are initiated by enabling the word-line (WL). To do write operation the value to be written is applied to the bit lines and for browse operation each BL and BLB is recharged to VDD. Whenever the browse operation the zero storing node is flustered & this might flip the keep data, but the palm write operation desires that information ought to be flipped terribly simply. Historically device size has been adopted to balance the browse versus write style needs.

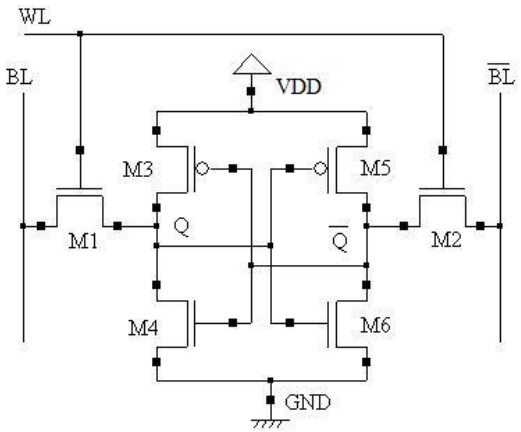


Fig1. *Conventional 6T SRAM*

The 6T SRAM cell design consists of two access transistors and two cross coupled CMOS inverters. Bit lines are the input/output ports of the cell with high capacitive loading. The operations READ and WRITE are conducted by these bit lines only; we will see how these are carried out. Write style needs.

A 6T SRAM cell consists of 2 cross-coupled CMOS inverters and 2 NMOS access transistors. The output (input) of the inverters construct the internal nodes of the cell A and B. Once active, the access transistors facilitate the communication of the cell internal nodes with the input/output ports of the cell. The input/output ports of the cell unit of measurement called bit lines (BL and BL.) Bit lines unit of measurement a shared data communications medium among the cells on an {analogous the same} column in an array of cells. Consequently, they need high physical phenomenon loading. The browse and write operations unit of measurement conducted through the bit lines as we tend to are reaching to see inside the long run sections.

2.2. Read Operation

Figure 1 illustrates the operation of the cell throughout a browse access. During this design, node node a carries a logic `zero' and node B carries a logic `one' before the cell is accessed. Thus, the transistors, M3 and M6, measure `off' whereas M4 and M5 live 'on' and catch up on the escape current of power supply and M6. In In customary vogue, the bit lines are precharged to VDD before the browse operation begins. An SRAM cell during read operation

Enabling of the word lines (WL), i.e., the gate of the access transistors starts the read operation. Because the word lines go high, power provide goes to saturation region whereas M4 operates in thermionic vacuum tube region. Attributable to the short-channel impact, this associated with power provide encompasses a linear relationship with the voltage of the node `A'. Hence, these transistors behave sort of a resistance throughout this operation. Therefore, power provide and M4 A resistance and elevate node `A' voltage by ΔV.

This voltage drives the input of the convertor M5-M3. to confirm CMOS SRAM: a outline sixteen a non-destructive browse operation ΔV is chosen such it does not trigger the M5-M3 electrical

converter and node B remains at VDD over the whole cell interval. Having a seamless voltage of VDD at the gate of M4 warrants the constant resistance assumption for M4 over the interval.

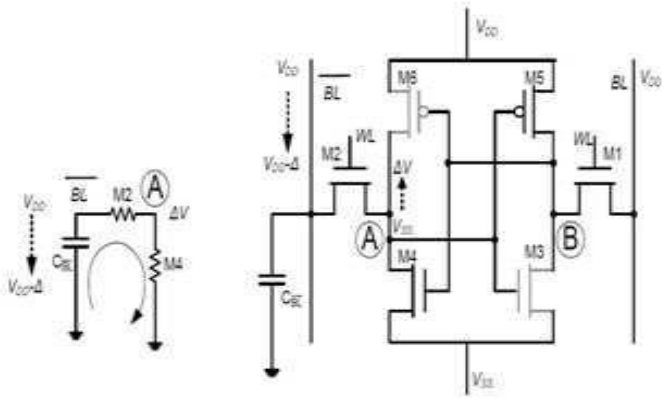


Fig2. *An SRAM Cell during Read operation*

Figure 2 shows the linear model of the bit line discharge path. Throughout this model the bit line capacitance of CBL is pre-charged to VDD. Upon the activation of power offer, CBL discharges through power offer and M4 and causes a free fall of ¢ on BL. Since the gate supply voltage of M1 remains at zero volts (i.e., Vgs1 = 0V), CBL cannot discharge and remains at VDD. The regardful voltage between BL and BL, ¢, is amplified using a way electronic equipment to supply the regular logic levels.

Clearly, a faster bit line discharge is achieved by reducing the resistance at intervals the discharge path. However, such enhancements return at the price of larger cell semiconductor device sizes that may not urged for prime density SRAMs.

DC analysis of the operation of the cell transistors is conventionally adopted to substantiate the soundness of the cell throughout the browse operation. as a result of it had been mentioned before, an occasional enough ΔV ensures that the output of inverters M5-M3 remains constant at node B. to make sure a non-de structive browse operation, the voltage level ΔV is controlled by the resistive magnitude relation of power provide and M4.

2.3. Write Operation

Figure 3.3 illustrates the operation of the cell inside the write operation. Throughout this figure the initial conditions of nodes A and B unit VSS and VDD, severally. Re-writing the recent data to the cell is trivial thus we have a tendency to tend to focus on propellant the knowledge of the cell.

In different words, the write operation is complete providing the voltage level on node A and B becomes VDD and VSS, severally. The activation of the word line cannot cause a spare voltage increase on node A to trigger the CMOS inverter M5-M3 if every bit lines unit of measurement pre-charged to VDD.

Therefore, the write operation is conducted by reducing the bit line associated with node B, BL, to a sufficiently low voltage (e.g., VSS.) This operation forms a possible divider comprising of M5 and power offer at the beginning of the operation.

To assess the voltage that appears at node B upon activation of the word lines in write operation, ΔV. A sufficiently low ΔV triggers the convertor M6-M4 that lands up in charging up node A to VDD. Since node a drives the convertor M5-M3, node B is force all the approach right down to VSS through power offer and M5 turns off. Hence, the logic state of the cell is changed. The word line becomes inactive once the completion of the operation. A in write operation ar usually bonded by choosing an accurate PR. A lower PR lands up during a lower ΔV, and a lower ΔV is expounded to higher drive at the input of convertor M6-M4.

3. 8T SRAM CELL

It is noteworthy that for associate SRAM cell, the specified form of operation is commonly set with the correct choice of the bit line voltage. However, this involves additional edge circuits like bit line precharge circuits and writes drivers to create positive correct bit line voltage setting before any

operation. At low provide voltages due the soundness limitations of 6T SRAM cell we tend to use 8T SRAM cell for quick transmission applications. it's like 6T SRAM cell with a scan decoupled path that consists of M5 and M6 transistors. Allow us to see the operating of 8T SRAM style.

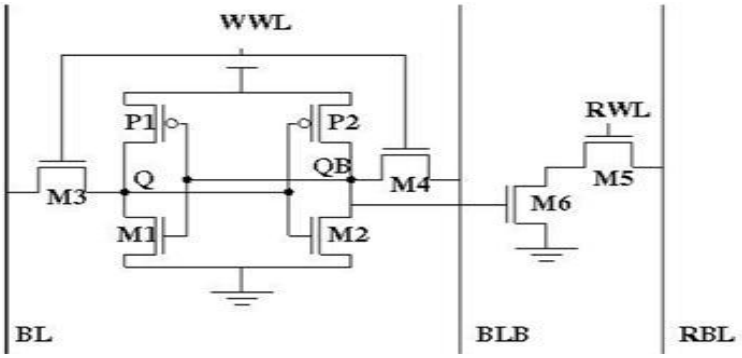


Fig3. *8T SRAM Cell*

3.1. Write Operation

The write operation of 8T SRAM cell is same as to the conventional 6T SRAM. The write operation in 8T SRAM is carried out as shown and discussed below

3.2. Write '0' Operation

For writing '0', the bit line has to give zero volts and VDD to the bit line (BLbar). And write word line is asserted which makes both the transistors M3 and M4 ON. Hence the value in the bit line is stored at Q. Hence '0' is stored at Q.

3.3. Write '1' Operation

Likewise writing '1' is also carried in the likely same. The bit line has to give a value VDD and bit line bar is given a value 0 volts. As WWL is enabled for write operation, the values in bit lines are store at respective nodes that is at Q will have value logical '1' and logical '0' at Qbar. There is no change in the write operation when compared with the basic SRAM operation.

3.4. Read Operation

The read operation is initiated by pre-charging the read bit line to VDD which is required in the conventional one.

3.5. Read '0' Operation

Read word line (RWL) drives the access transistor M5 ON. If the value stored at Q is '0' then transistor M6 will be ON and RBL is connected to ground directly through M5&M6 transistors discharges. This implies that the value stored at Q in the SRAM is zero.

3.6. Read '1' Operation

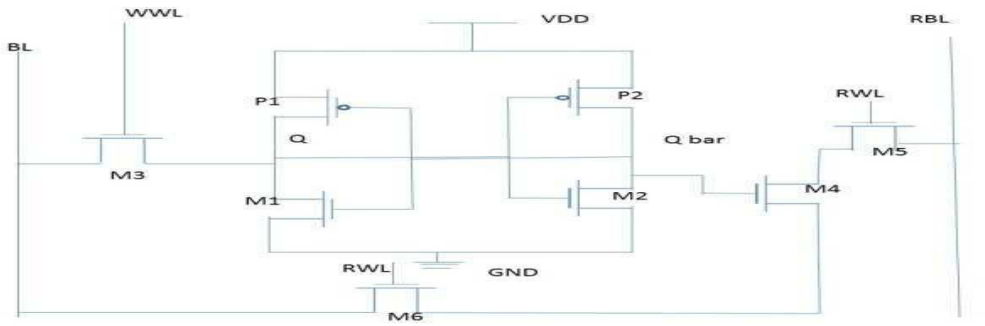
If the value stored at Q is '1', due to M6 transistor will be OFF and there is no discharge path for RBL, and the value in RBL is VDD which shows that value stored at Q is '1'. The circuit diagram of 8T SRAM shown in the figure 4.

The disadvantages in 6T SRAM are minimized in 8T SRAM, even though the transistor count increased the power consumption. The circuit diagram and operations of conventional and 8T SRAM are discussed in this chapter. The SRAM with charge sharing concept is discussed next.

4. PROPOSED SRAM DESIGN

Here the proposed SRAM design is using the concept of charge sharing of 10T SRAM design. But the difference is that the design is done with less number of transistors when compared to the above 10T SRAM which also decreases the area of the design and in the proposed design we also reduced the power consumption when compared with the previous design.

The proposed SRAM consists of a single ended 7T bit cell which has one bit line (BL) for write operation and one Read Bit cell for read operation.



During the write operation WWL was enabled and RWL was disabled (i.e RWL='0') so M4 M5 M6 are in the off state. The cell acts like single ended 5T SRAM Cell and writes the Bit line data into the cross coupled inverter pair P1 M3 and P2 M2.

During the read operation the bit line disconnected from inverter pair because of WWL='0' during read phase and RWL was enabled so M6 M5 will be in the ON state. For read operation here we are using separate bit line called RBL instead of using same BL. SO during read operation RBL was pre-recharged.

Read '0': In reading '0' M4 was ON state, so RBL has a discharging path from M4 M5 and M6, the M6 will acts like a charge sharing network, instead of discharging the charge to the ground M6 will charge the bit line (BL) so there will no loss of power to the ground.

Read'1': In reading '1' M4 was OFF state so there will be no discharging path for RBL to discharge maintains the charge and reads the '1'

5. SIMULATION AND RESULTS

These SRAM designs are designed and simulated using S-edit and T-Spice using TSMC018 technology in Tanner Tools 13.0. The Conventional 8T SRAM, and Proposed SRAM are simulated there power dissipations are compared and shown in below:

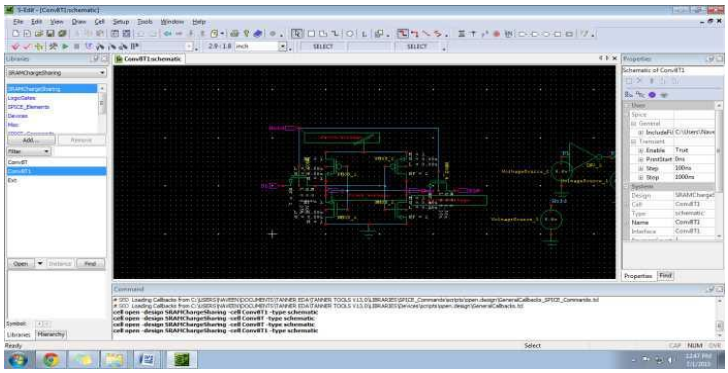


Fig5. *S-edit Design of 6T SRAM Cell*

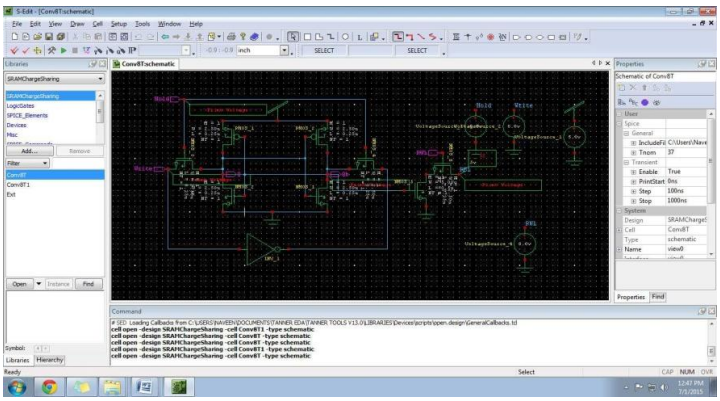


Fig6. *S-edit Design of 8T SRAM Cell*

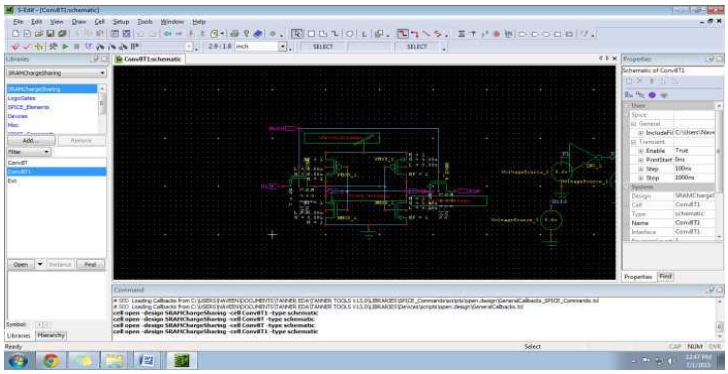


Fig7. *S-edit Design of Proposed SRAM Cell*

Circuit	Power Consumption
Conventional 6T SRAM	5.517330e-004 watts
8T SRAM Cell	9.461892e-010 watts
Proposed SRAM Cell	5.806951e-010 watts

6. CONCLUSION

Here we have used the designs of SRAM of charge sharing and analyzed the design for minimum area and power as well. The design technique will reduce power and maintain at good stability levels.

7. FUTURE SCOPE

In future we can extend this multi bit SRAM Cells and overall bit line discharge losses can be reduced by using adiabatic logics.

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AUTHOR'S BIOGRAPHY

Lingam Rajesh, Completed B.TECH in SREE Rama Eng College (ECE) (JNTU-A), M.TECH Mallareaddy Eng College (VLSISD) Hyderabad, Area of Interest: VLSI System Design.

Santosh J, Assistant Professor in ECE At MREC, Completed B.TECH: CVR College Of Eng. JNTU-H, M.TECH: VLSI System Design, SDES, JNTU-H Area of Interest VLSI System design Reconfigurable Archicture & Design of Fault Tolerant Systems.