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MSIC Pattern Generation Using LFSRs

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Abstract: *Testing in VLSI circuit is difficult due to the many challenges as a rapid growth in design complexity. These challenges include the power dissipation and test application time within particular limit of time. Actually in basic LFSR power consumption is high. This paper is proposed method to existing Bit Swapping and Low Power Linear Feedback Shift Register. This paper explains the Automatic test pattern generation on Built in Self Test. In ordinary LFSR the random test vectors can be generated but the power consumption is high because of more number of transitions. The modified LFSR's are BS-LFSR and LP-LFSR. To overcome this ordinary LFSR disadvantage the existing LP-LFSR and BS-LFSR are used. Here we are using twisted ring counter and level generator.TPS and TPC are implemented using these. Here we are using the benchmark circuit , C432 as a DUT. Here, both TPC and TPS are done by using LFSR ,BS-LFSR and LP-LFSR. TPS with LP-LFSR and BS-LFSR is lower than the power during TPC. The power calculation is done in modelsim. This results show power reduced in respectively with different methods.*

Keywords: *LFSR,LP-LFSR,BS-LFSR,TPS,TPC,DUT*

1. INTRODUCTION

A Digital system is tested and diagnosed during its lifetime on numerous occasions. Test a diagnosed must be quick and very fault coverage. One way to ensure this is to specify test as one of the system function, so it become self test. There are number of techniques for generating the test pattern.the oldest method is LFSR. In ordinary LFSR[1] the pseudo random patterns that are generated,the switching transitions are high.Hence the dynamic power is also high. To overcome this the proposed theory LP-LFSR[27] and BS-LFSR[24] are used.In LP-LFSR,by using R-injectors and dividing bits into two groups based on the state machine operation we can reduce almost 50% of transitions than in LFSR.In BS-LFSR,the output from the LFSR are swapped so that the transitions are reduced to 33% than in LFSR.There are two test applications in BIST. They are Test per clock and test per scan[8]. In this Test per clock scheme the output of a TPG directly feed the input of the CUT, and the output of the CUT is directly connected to MISR. In the test per scan, the name itself indicates the test patterns are captured into the san chain. The main advantage of this scan based testing is its lower hardware are overhead while the main disadvantage is test application time.

2. BACKGROUND WORK ON BIST

Frohwerk ushered[2] is a new decade for determining the circuit accuracy by examining the signature, which is some standards of a circuit. He applied this experiment on Peterson[3] and Weldon[4] on error correcting codes and shift register to Built in self test(BIST). The transition count and bist to determine whether the signature circuit is good or bad can be analyse by the frohwerk. Mostly digital system can be tested at the T&T labs in 1987 had self test on the software. This is having a disadvantages these are the it took long time to test when we are testing coplex circuit. This statement shows software testing is slow,long and expensive to develop.Because of this researchers found build the self test function on the hardware. This is also providing the costly prototyping turns. Several advanced BIST[26] techniques have been studied and applied. The first class is the LFSR tuning. Girard et al.Analyzed the impact of an LFSR's polynomial[5] and seed Selection on the CUT's switching activity, and proposed a method to select the LFSR seed for energy reduction. The second class is low-power TPGs. One approach is to design low-transition TPGs. Wang and Gupta used two LFSRs of different speeds to control those inputs that have elevated transition densities.

2.1 Overview of Modified LFSR's

A.BS-LFSR

Bit swapping LFSR is modified LFSR. Addition of MUX along with conventional LFSR constitutes BS-LFSR. The number of transitions are reduced when compared with the conventional LFSR[24]. The fig.1.shows the 4 bit BS-LFSR.A common clock signal is given to a series of Flip Flops as control signal.Mux are used for swapping the outputs of the D-FFs

The output of the last FF is taken as the selection line for all the FFs.

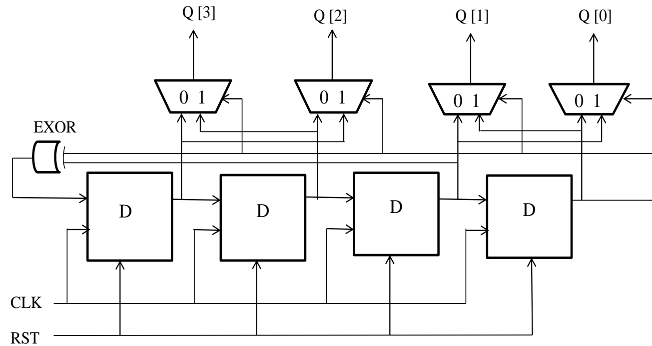


Fig1. *4-bit BS-LFSR*

If the output of the last FF is '0', then the output Q[3:0] is same as the output of all the FFs. If the output of the last FF is '1', then swapping of the outputs of the adjacent FFs is done. In conventional LFSR,the no.of transitions would be 2n-1.In BS-LFSR,the no.of tranisitions are 2n-2.Thus 50% of transitions are reduced.

B. Low Power LFSR

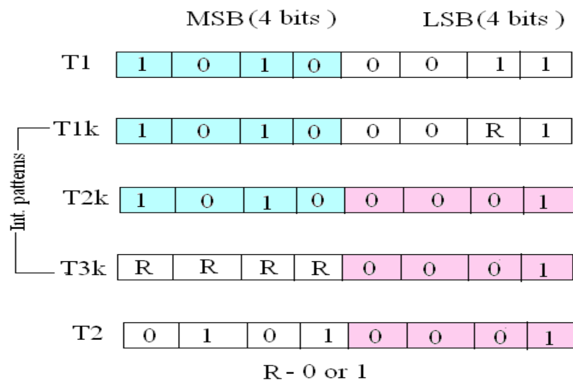


Fig2.*Producing intermediate patterns*

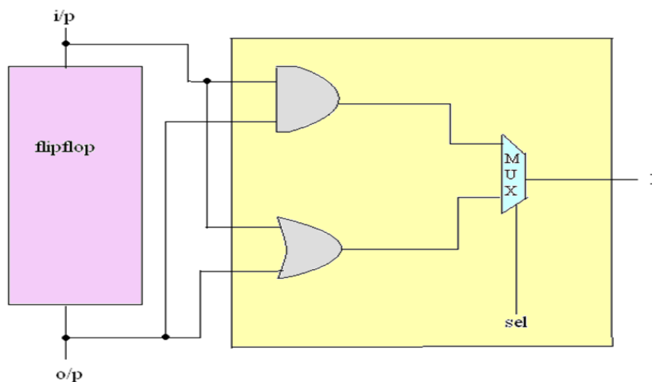


Fig3. *RI circuit*

In this method, we introduce three intermediate patterns between two consecutive sequences [31]. Here T1K, T2K and T3K are three intermediate patterns. The value of R can be generated by using RI circuit which is shown in Fig.3.As shown in Fig.2.T1 –input sequence.T2—right shift of T1.T1k,T2k,T3k—intermediate sequences.T2k--1st half of T1+2nd half of T2.T1k-first half of

T1+comparison between T1 &T2k.If bits are similar then same bits will be retained otherwise last bit of T1 is positioned. T3k—first half is the comparison between T2k &T2 + 2nd half of T2.

3. PROPOSED SIC GENERATION

This section develops a TPG[26] scheme that can be converted a one bit change pattern to unique low transition vectors for different scan chains. First, one bit change pattern is decompressed to its multiple codeword's. This means the Twisted ring counter[6] initially generated a particular bit pattern and this is xored with the seed generator output.These exored bits are stored individually in different scan chains. This operation continues till the 2n counter patterns are generated. The proposed MSIC-TPG consists of a Twisted ring counter, a seed generator, an XOR gate network, and a clock and control block.As well as , the generated code words will bit-XOR with a same seed vector in turn. Hence, a test pattern with similar test vectors will be applied to all scan chains.

A.TPG Method

There are m primary inputs (PIs) and M scan chains in a full scan design, and each scan chain has scan cells. The vector generated by an m-bit LFSR with the primitive polynomial can be expressed as the equation is the S(t) = S0(t)S1(t)S2(t), . . . , Sm−1(t) (hereinafter referred to as the seed), and the vector generated by an l-bit moebius counter can be expressed as M(t) = M0(t)M1(t)M2(t), . . .Ml−1(t).The first clock cycle of , *M is = M*0 *M*1 *M*2*, . . Ml*−1 will bit-XOR with *S = S*0*S*1*S*2*, . . . , SM*−1, and the results *F*1*Fl*+1*F*2*l*+1*. . . F(M*−1*)l*+1 will be shifted into *M* scan chains, respectively. In the second clock cycle, *M = M*0*M*1 *M*2*, . . . , Ml*−1 will be circularly shifted as *M = Ml*−1 *M*0 *M*1*, . . . , Ml*−2, which will also bit-XOR with the driver circuit equation is the *S*= *S*0*S*1*S*2*, . ,SM*−1. The resulting *X*2*Xl*+2*X*2*l*+2*, ., . . X(M*−1*)l*+2 will be shifted into *M* scan chains respectively. After *n* clocks, each scan chain will be fully loaded with a unique twisted codeword, and seed *S*0*S*1*S*2*. Sm*−1 will be applied to *m* PIs. Therefore circular twisted ring counter can generate *n* unique twisted code words through circular shifting the twisted

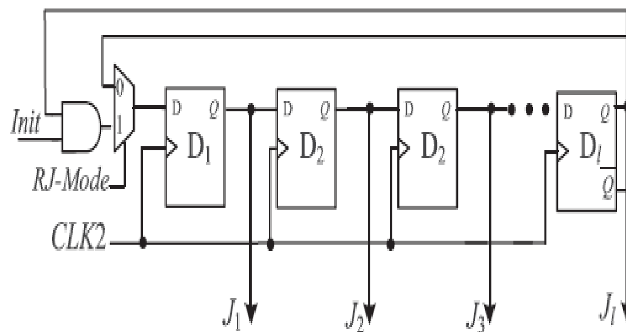


Fig.4*Reconfigurable Twisted ring counter*

vector, the circular twisted ring counter and XOR gates.

B. Reconfigurable Twisted ring counter

As shown in Fig. 4(a), it can operate in three modes. Mainly the reconfigurable means the patterns initial value is "reconfig". Normal twisted ring counter 000 pattern is not possible but using this we can implemented.

Table1. *Modes of RTRC*

Mode	RJ_mode	Init	Operation
Start	1	0	Counter is initialized to all 0's by clocking more than n times
Circular shift	1	1	Gives output code by clocking n times
Normal	0	1	2n unique SIC vectors by clocking 2n times

4. MULTIPLE SIC SEQUENCE

The proposed algorithm is to reduce the switching activity. In order to reduce the hardware overhead, the linear relations are selected with consecutive vectors or within a pattern, which can generate a sequence with a sequential de compressor, facilitating hardware implementation. Another requirement

is that the MSIC sequence should not contain any repeated test patterns, because repeated patterns could prolong the test time and Reduce test efficiency.

A. MSIC-TPGs for Test-per-Clock Schemes

The MSIC-TPG for test-per-clock schemes is illustrated in Fig. 5. The CUT's PIs $X1 - Xmn$ are arranged as an $n \times m$ SRAM-like grid structure[14]. Each grid has a two-input XOR gate whose inputs are tapped from a seed output and an output of the Johnson counter. The outputs of the XOR gates are applied to the CUT's PIs. A seed generator is an m-stage conventional LFSR, and operates at low frequency Clock1. The test procedure is as follows.

1) The seed generator generates a new seed by clocking Clock1 one time.
2) The twisted ring counter generates a new vector by clocking Clock2 one time.
3) Repeat 2 until $2n$ twisted vectors are generated.
4) Repeat 1–3 until the expected fault coverage or test length is achieved.

B. *MSIC-TPGs for Test-per-Scan Schemes*

The MSIC-TPG for test-per-scan schemes is illustrated in Fig.6. The stage of the SIC generator is the same as the maximum scan length, and the width of a seed generator is based on 3 conditions.

1) The seed circuit generates a new seed by clocking CLK1 one time.

2) M0 is set to "0". The reconfigurable twisted ring counter will operate in the Twisted ring counter mode and generate a Twisted vector by clocking CLK2 one time.

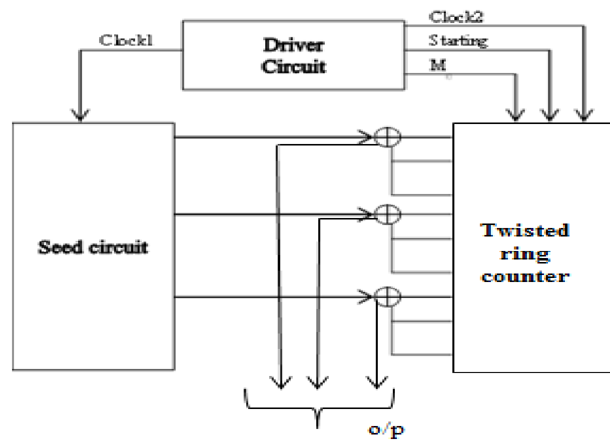


Fig5. *Test per Clock Scheme*

3) After a new Twisted vector is generated, M_0 and start are set to 1. The reconfigurable Twisted ring counter operates as a circular shift register, and generates n codewords by clocking CLK2 n times. Then, a capture operation is inserted.
4) Repeat 2–3 until $2n$ Twisted vectors are generated.
5) Repeat 1–4 until the expected fault coverage or test length is achieved.

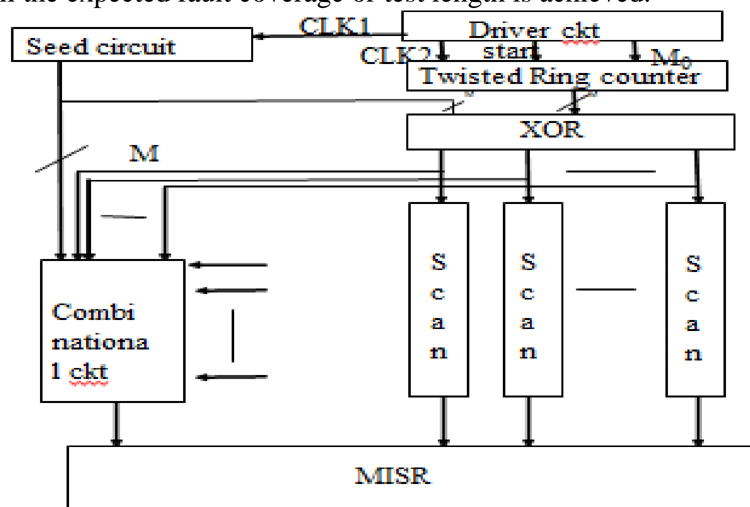
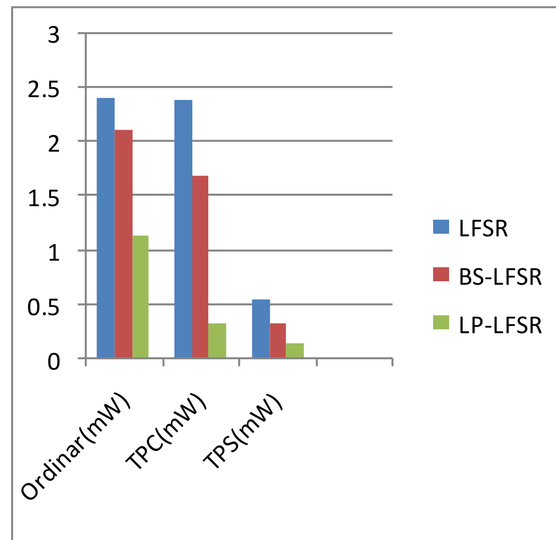


Fig6. *(a) Test Per Scan scheme*

5. Result and Analysis



We observe that dynamic power is less for TPS with LP-LFSR compare with ordinary and other TPC modules.-LFSR almost 80 % of dynamic power is reduced.

6. Conclusion

This paper has proposed a low power test pattern generation method that could be easily implemented easily on the hardware. The number of applying test vectors plays a crucial role and reduced applying test vectors time respectively. This is possible with the combination of Twisted ring counter and modified LFSRs. By using this we easily implemented the MSIC-test pattern generation. This can be done by using two methods, Test Per Clock and Test Per Scan. Mostly Test Per Clock is best but for applying the patterns Test Per Scan is better. The experiment results analyse the Test Per Scan reduces the area overhead and become more accuracy.

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