International Journal of Innovative Research in Electronics and Communications (IJIREC)
Volume 2, Issue 5, July 2015, PP 45-54
ISSN 2349-4042 (Print) & ISSN 2349-4050 (Online)
www.arcjournals.org

A 5v 124mw 64 – Bit Advanced Comparator for DSP Processor

T.Mounika
M.Tech (VLSI SYSTEM DESIGN)
Vaagdevi College of Engineering
Warangal, India
thtmounika@gmail.com

P.Prasad Rao
HOD, Department of ECE
Vaagdevi College of Engineering
Warangal, India
prasadrao_hod@yahoo.co.in

Abstract: *A 5V, 124mw 64 bit Advanced Comparator for DSP Processor is proposed in this paper. This paper briefly presents comparison of the modified and existing 64 - bit binary comparator designs, which allows reducing power consumption and delay. Some modifications have done in existing 64- bit binary comparator design to improve the performance of the circuit. Comparison between modified and existing 64 – bit binary comparator designs is calculated by simulation that is performed in Tanner EDA Tool.*

Keywords: *Binary comparator, comparison, high speed, low power, performance.*

1. INTRODUCTION

The comparison of two numbers is one of the arithmetic operation in which one number is greater than, equal to or less than the other number. An n-bit Magnitude comparator is a combinational circuit that compares n- inputs of A with the n- inputs of B and determines their relative magnitudes as in Fig. 1. The output of the comparison is given by three binary values that gives whether A>B, A<B, or A=B. The circuit used for comparison of two n-bit numbers has 2n inputs and 2^ 2n entries in the truth table. For 2 bit numbers, it has 4- inputs and 16- rows in the truth table; similarly, for 3- bit numbers 6-inputs and 64-rows in the truth table [1].

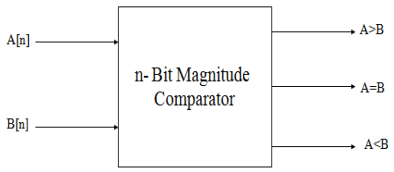

Fig1. *Block diagram of the n- bit Magnitude Comparator.*

In the recent years, high speed & low power devices have been emerged in the electronic industry due to increasing demand of the portable devices. This tremendous increase in demand is due to popularity of battery operated portable equipments such as personal computing devices and medical applications in which high speed and small power consumption are considered.

Depending upon the logic style chosen the speed, size, and power dissipation and wiring complexity of the circuit varies, circuit size depends upon the number of transistors and their sizes. The wiring complexity [2] is determined by number of connections and their lengths and by which single rail or dual rail logic is used. Power dissipation is given by the switching activity and the node capacitances. All these characteristics may vary from one logic style to another and thus the proper choice of logic style is done for the crucial performance.

In order to difference both the designs existing and modified simulations are done for delay and power consumption with 5.0 volt input voltage (supply voltage), 25°C temperature in Tanner EDA Tool.

2. 64 - BIT BINARY COMPARATOR

The 64 – bit binary comparator has inputs (A63 to A0 & B63 to B0).This 64 bits of each A and B are used for comparison. For performing this comparison truth table has 128 inputs & 2^128 entries. This

can be designed with the help of tree based structured logic by using minimum number of bits a comparator of maximum number of bits can be designed [5],[6],[7],[8].

3. EXISTING 64 - BIT BINARY COMPARATOR DESIGN

The 64 - bit comparator design with reference to [8], [9], [10] gives tree- based structure, it consists of G (generate) and P (propagate) signals for performing binary additions. For two numbers each having A1, A0 & B1, B0 the comparison can be performed by:

$$B_{Big} = \overline{A_1}\ B_1 + \overline{(A1 \oplus B_1)}\ .\ \left(\overline{A_0}\ B_0\right) \quad (1)$$

$$EQ = \overline{(A_1 \oplus B_1)}\ .\ \overline{(A_0 \oplus B_0)} \quad (2)$$

Where B_{Big} is defined as the output for (A_LT_B). For A<B, "$B_{Big, EQ}$" is "1, 0". For A=B, "B_{Big}, EQ" is "0, 1".Hence for A>B, "B_{Big}, EQ" is "0, 0". Equation"(1)" gives that it is same as the carry signal generated in the binary additions.

Consider for the carry generation as:

$$C_{out} = AB + (A \oplus B)\ .\ C_{in}$$

$$= G + P.\ C_{in} \quad (3)$$

Where A & B are the binary inputs, C_{in} is the carry signal, C_{out} is the carry output signal. G and P are generate & propagate signals. After comparison of (1) & (3):

$$G_1 = \overline{A_1}\ B_1 \quad (4)$$

$$EQ_1 = \overline{(A_1 \oplus B_1)} \quad (5)$$

$$C_{in} = \left(\overline{A_0}\ B_0\right) \quad (6)$$

C_{in} can be considered as G_0. For Static logic, (1) requires big transistor stack height, so an encoding scheme is used and given as:

$$G_{[i]} = \overline{A_{[i]}}\ B_{[i]} \quad (7)$$

$$EQ_{[i]} = \overline{(A_{[i]} \oplus B_{[i]})} \quad (8)$$

Where i=0……..63. Put the values of "(7)" & "(8)" in "(1) & (2)".

$$B_{Big[2j+1:2j]} = G_{[2j+1]}\ .\ G_{[2j]} \quad (9)$$

$$EQ_{[2j+1:2j]} = EQ_{[2j+1]}\ .EQ_{[2j]} \quad (10)$$

Where j=0……..31.G & P signals are combined to form group of G & P signals.

$$B_{Big\,[3:0]} = \overline{A_3}\ B_3 + \overline{(A_3 \oplus B_3)}\ .\ \left(\overline{A_2}\ B_2\right) + \overline{(A_3 \oplus B_3)}\ .\ \overline{(A_2 \oplus B_2)}.\ \left(\overline{A_1}\ B_1\right)$$

$$+ \overline{(A_3 \oplus B_3)}.\ \overline{(A_2 \oplus B_2)}.\ \overline{(A_1 \oplus B_1)}.\ \left(\overline{A_0}\ B_0\right)$$

$$B_{Big\,[3:0} = \left(\overline{A_2}\ B_2\right) + \overline{(A_2 \oplus B_2)}\ .\ [\left(\overline{A_2}\ B_2\right) + \overline{(A_2 \oplus B_2)}\ .\ \{\overline{A_1}\ B_1 + \overline{(A_1 \oplus B_1)}.\ \left(\overline{A_0}\ B_0\right)\}]$$

$$B_{Big[3:0]} = G3 + EQ_3.\ \{G_2 + EQ_3\ .\ (G_1 + EQ_1\ .\ G_0)\}$$

$$B_{Big[3:0]} = B_{Big[3:2]} + EQ_{[3:2]}\ .\ B_{Big[1:0]} \quad (11)$$

$$EQ_{[2:0]} = EQ_{[3:2]}\ .\ EQ_{[1:0]} \quad (12)$$

Similarly for the 64 – bit comparator, B_{Big} & EQ can be given as:

$$B_{Big[64:0]} = G_{64} + \sum_{k=0}^{62}\left(G_K\ .\ \prod_{m=k+1}^{63} EQm\right) \quad (13)$$

$$EQ_{[3:2]} = \prod_{m=0}^{63} EQ_m \quad (14)$$

Fig. 2. Shows the tree diagram of 8- bit binary comparator and Fig. 3. – Fig. 5. Shows corresponding schematic for each block of each stage. In 8- bit circuitry, the first stage comparison circuit implements "(9)" & "(10)" for j=0…3, whereas the second stage generates $B_{Big[3:0]}$,$B_{Big[7:4]}$ and $EQ_{[3:0]}$, $EQ_{[7:4]}$ according to "(11)" & "(12)". Finally $B_{Big[7:0]}$ and $EQ_{[7:0]}$ are calculated in third stage according to "(13)" & "(14)".

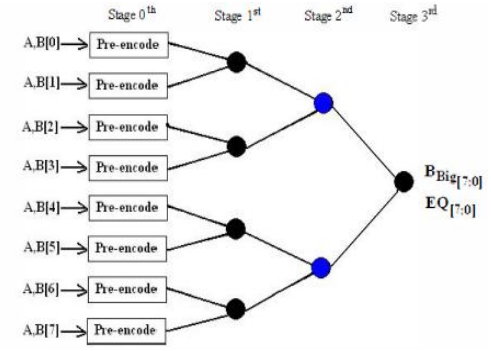

Fig2. *Tree diagram of the 8- bit Binary Comparator.*

In 0^{th} stage modified pass transistor logic style circuit as in Fig. 3 is employed to produce "less than" & "equal to" outputs.

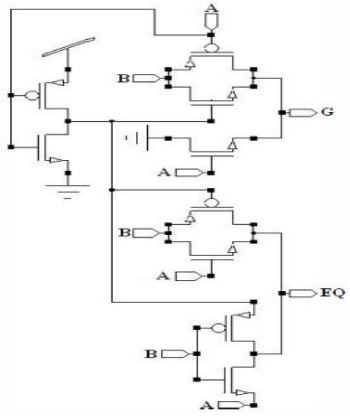

Fig3. *Schematic of the Stage 0^{th} of Existing 64 – Bit Binary Comparator.*

In 1^{st} stage CMOS circuitry as in Fig. 4 is employed to produce inverse inputs for stage 2^{nd}.

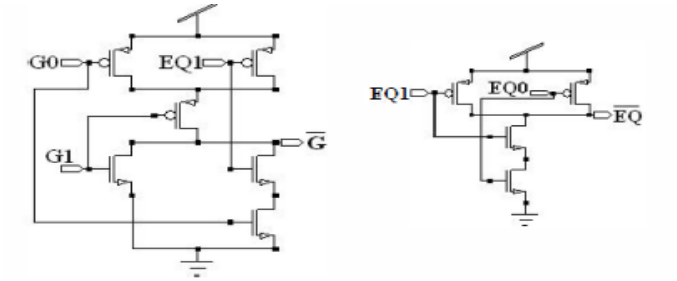

Fig4. *Schematic of the Stage 1^{st} of Existing 64 - Bit Binary Comparator.*

In 2^{nd} stage again CMOS circuitry as in Fig. 5 is employed to produce actual inputs for stage 3^{rd}.

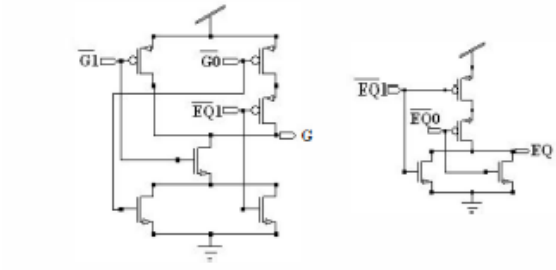

Fig5. *Schematic of the Stage 2^{nd} of Existing 64 - Bit Binary Comparator.*

The 64- bit comparator is designed by using 7 stages from 0^{th} to 6^{th} as in (Fig.6). According to the tree structure given in the Fig.2, the circuitry of stage 1^{st} is used for the stage 3^{rd}. Similarly for the stage 4^{th} circuitry of 2^{nd} stage is employed. For stage 5^{th} circuitry of 1^{st} stage is employed. For stage 6^{th} circuitry of stage 2^{nd} is employed. By following this schematic of 64 - bit binary comparator is drawn and shown in Fig.6. Description about this design is given in Table. 1. Existing design requires 2072 transistors for 64- bit binary comparator.

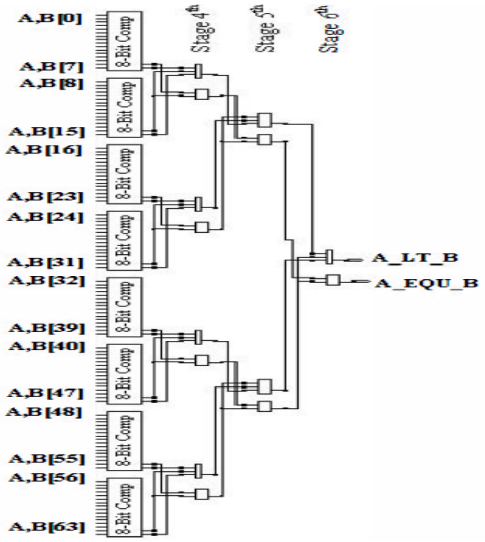

Fig6. *Schematic of the Existing 64 - Bit Binary Comparator.*

According to the input bit stream, waveforms of the existing 64 – bit binary comparator are obtained and shown in the Fig.7. Waveforms describes that only one output is high ("1") at a time. When both outputs "A less than B" & "A equal to B" (A_LT_B & A_EQU_B) are low ("0") then the waveform represents that "A greater than B" output is high (A_GT_B) is "1".Simulation results following this design are given in Table.3 for conclusion.

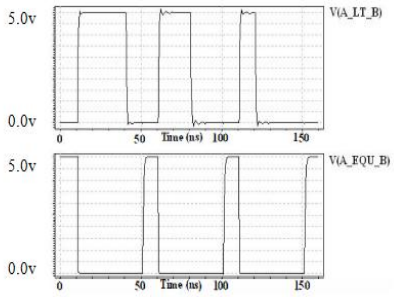

Fig7. *Waveforms of the Existing 64 - Bit Binary Comparator.*

4. MODIFIED 64 – BIT BINARY COMPARATOR DESIGN

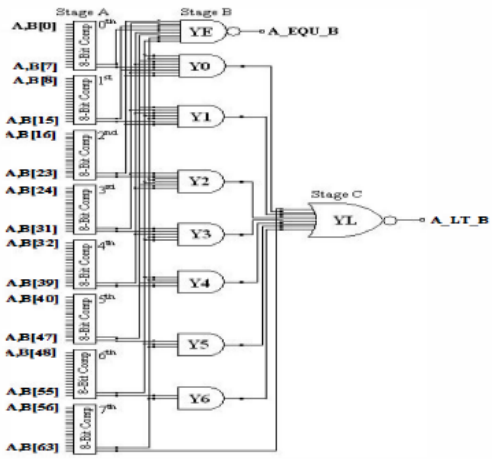

Fig8. *Logic Diagram of the Existing 64 - Bit Binary Comparator.*

Some modifications have done in the existing binary comparator design [8] to decrease the power, delay and power – delay product of the circuit to achieve high performance. The Existing 64 – bit binary comparator design [8] follows tree-based structure from 2-bit to 64- bit circuitry but modified design follows tree - based structure from 2- bit to 8 – bit circuitry. Fig.8. shows logic diagram of the modified 64 – bit binary comparator design.

In the modified design three stages are used. In stage A eight 8 – bit comparators are used to provide "A less than B" and "A equal to B" outputs. In stage B NAND gate is used to provide "A equal to B" output and AND gates have been used to provide input for stage C. In stage C NOR gate is used to provide "A less than B" output. Description about this design is given in tabular form in Table. 2.

In stage B "A less than B" output of 0^{th} stage of 8 – bit comparator and "A equal to B" outputs of seven from (1^{st} to 7^{th}) 8 – bit comparators are given to AND gate Y0 to produce input for NOR gate YL. This 8- input AND is implemented by using GDI logic style. Multiple - input gates are implemented by combining several GDI cells [11], [12].One 8 – input AND gate is implemented by using 14 transistors. The Schematic of the AND gate Y0 of modified 64 – bit binary comparator design is shown in Fig 9.

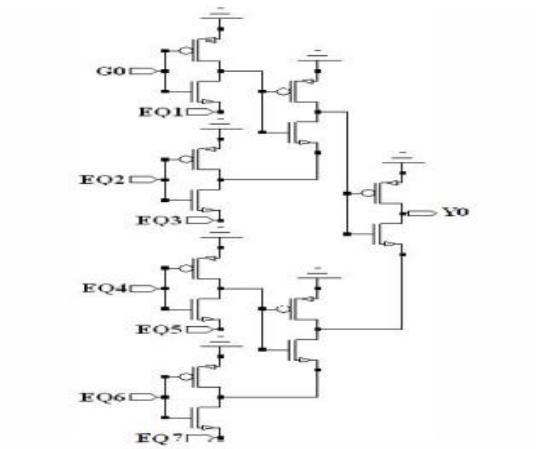

Fig9. *Schematic of the AND Gate Y0 of Modified 64 - Bit Binary Comparator.*

The "A less than B" output of 1^{st} stage of 8 – bit comparator and "A equal to B" outputs of six from (2^{nd} to 7^{th}) of 8 – bit comparators are given to AND gate Y1 to produce input for NOR gate YL. This 7- input AND gate is implemented by using GDI logic style. One 7 – input AND gate is implemented by using 12 transistors. The Schematic of AND gate Y1 of modified 64 – bit binary comparator design is shown in Fig.10.

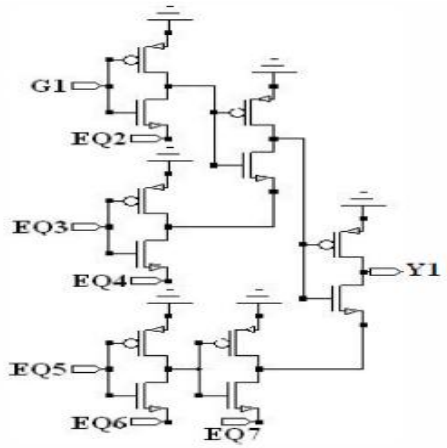

Fig10. *Schematic of the AND Gate Y1 of Modified 64 - Bit Binary Comparator.*

The "A less than B" output of 2^{nd} stage of 8 – bit comparator and "A equal to B" outputs of five from (3^{rd} to 7^{th}) of 8 – bit comparators are given to AND gate Y2 to produce input for NOR gate YL. This 6- input AND gate is implemented by using GDI logic style. One 6 – input AND gate is implemented by using 10 transistors. The Schematic of AND gate Y2 of modified 64 – bit binary comparator design is shown in Fig.11.

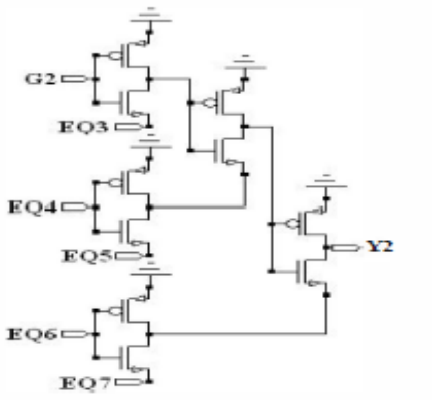

Fig11. *Schematic of the AND Gate Y2 of Modified 64 - Bit Binary Comparator.*

The "A less than B" output of 3rd stage of 8 – bit comparator and "A equal to B" outputs of four from (4th to 7th) of 8 – bit comparators are given to AND gate Y3 to produce input for NOR gate YL. This 5- input AND is implemented by using GDI logic style. One 5 – input AND gate has is by using 8 transistors. The Schematic of AND gate Y3 of modified 64 – bit binary comparator design is shown in Fig.12.

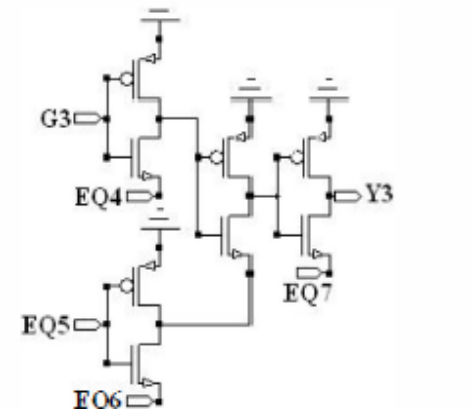

Fig12. *Schematic of the AND Gate Y3 of Modified 64 - Bit Binary Comparator.*

The "A less than B" output of 4th stage of 8 – bit comparator and "A equal to B" outputs of three from (5th to 7th) of 8 – bit comparators are given to AND gate Y4 to produce input for NOR gate YL. This 4- input AND gate is implemented by using GDI logic style. One 4 – input AND gate is implemented by using 6 transistors. The Schematic of AND gate Y4 of modified 64 – bit binary comparator design is shown in Fig.13.

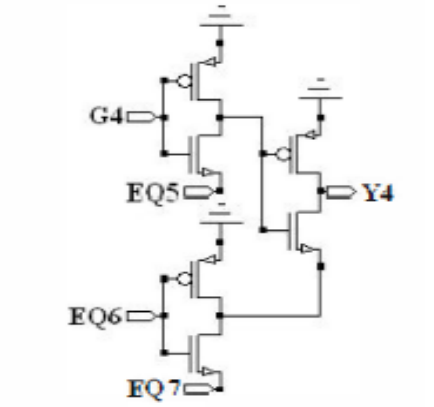

Fig13. *Schematic of the AND Gate Y4 of Modified 64 - Bit Binary Comparator.*

The "A less than B" output of 5th stage of 8 – bit comparator and "A equal to B" outputs of two from (6th to 7th) of 8 – bit comparators are given to AND gate Y5 to produce input for NOR gate YL. This 7- input AND gate is implemented by using GDI logic style. One 3 – input AND gate is implemented by using 4 transistors. The Schematic of AND gate Y5 of modified 64 – bit binary comparator design is shown in Fig.14.

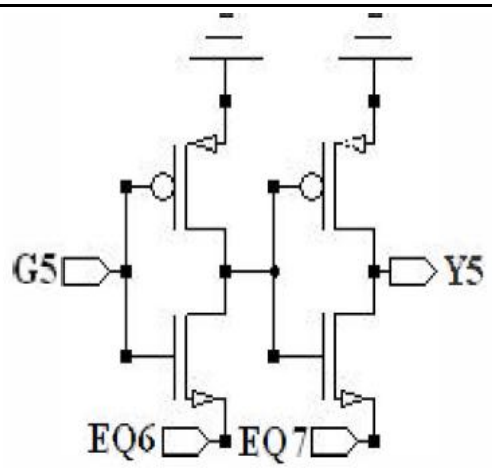

Fig14. *Schematic of the AND Gate Y5 of Modified 64 - Bit Binary Comparator.*

The "A less than B" output of 6^{th} stage of 8 – bit comparator and "A equal to B" output of 7^{th} of 8 – bit comparator is given to AND gate Y6 to produce input for NOR gate YL. This 2- input AND gate is implemented by using GDI logic style. One 3 – input AND gate is implemented by using 2 transistors. Schematic of AND gate Y6 of modified 64 – bit binary comparator design is shown in Fig.15.

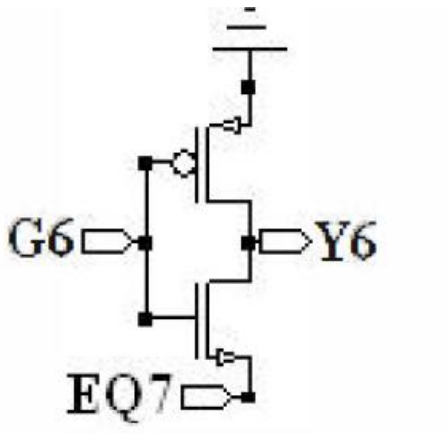

Fig15. *Schematic of the AND Gate Y6 of Modified 64 - Bit Binary Comparator.*

The "A equal to B" outputs of eight from (0^{th} to 7^{th}) of 8 – bit comparator are given to NAND gate YE to produce "A equal to B" output of modified 64 – bit binary comparator. This 8 – input NAND gate is implemented by using CMOS logic style. To avoid transistor stack height 8 – inputs are NANDed through four 2- input NAND gates then NORed through one 2 - input NAND gate. One 8 – input NAND gate is implemented by using 28 transistors. Schematic of NAND gate YE of modified 64 – bit binary comparator design is shown in Fig.16

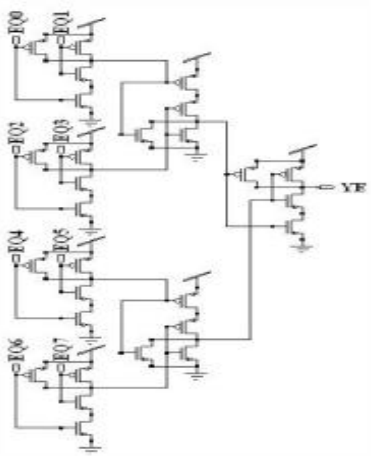

Fig16. *Schematic of the NAND Gate YE of Modified 64 - Bit Binary Comparator.*

In the stage C "A less than B" output of 7th stage of 8 – bit comparator and outputs of seven AND gates from (Y0 to Y6) are given to NOR gate YL that produces "A less than B" output of the modified 64 – bit binary comparator design. This 8- input AND gate is implemented by using GDI logic style. One 8 – input NOR gate is implemented by using 16 transistors. Schematic of NOR gate YL of modified 64 – bit binary comparator design is shown in Fig.17.

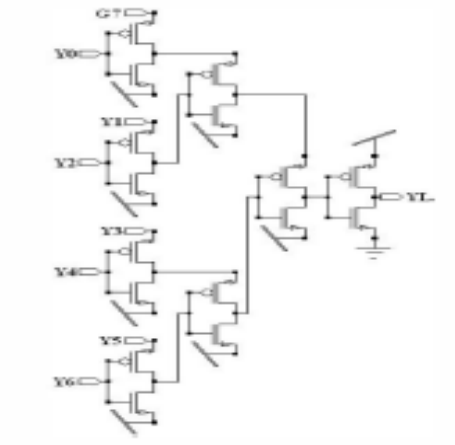

Fig17. *Schematic of NOR Gate YL of Modified 64 - Bit Binary Comparator.*

The output of 8- bit comparators are obtained in the inverse form so NOR and NAND gates are used in place of OR and AND gates that produces final output of "A equal to B" and "A less than B". This comparator design requires 1276 transistors for 64 – bit modified 64 - bit comparator. Schematic of modified 64 – bit binary comparator design is shown in Fig.18.

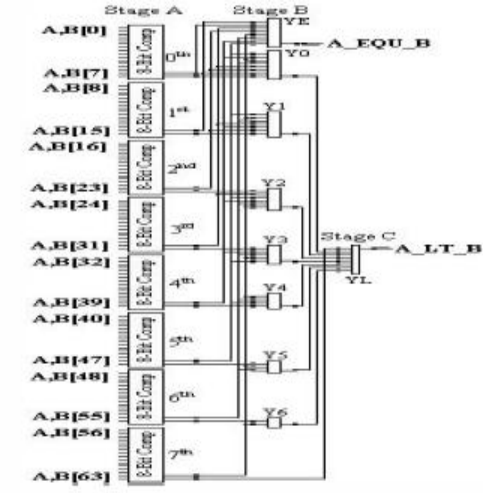

Fig18. *Schematic of the Modified 64 - Bit Binary Comparator.*

According to the input bit stream waveforms of the modified 64 – bit binary comparator are obtained and shown in the Fig.19. Simulation results of the modified 64 – bit binary comparator design is given in the tabular form in Table. 3.

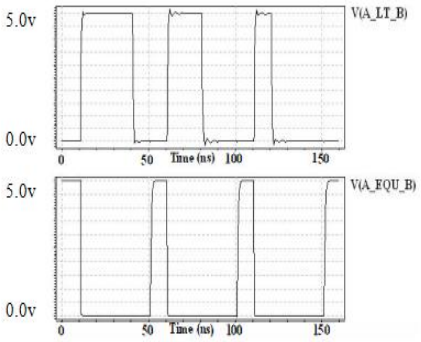

Fig19. *Waveforms of Modified 64 - Bit Binary Comparator.*

5. SIMULATION AND COMPARISON

After simulation of both the designs results are obtained for delay and power consumption and by taking product of delay, power consumption and power delay product is obtained and shown in Table 3. Simulations are carried in Tanner EDA Tool for both existing and modified 64 – bit binary comparator design.

Table1. *Description of Existing 64 – bit binary comparator design.*

Detail	Stage 0^{th}	Stage 1^{st}	Stage 2^{nd}	Transistor Count
Design	Using MPTL Style	Using CMOS style	Using CMOS style	2076
Nature of Output	Actual	Inverse	Actual	

Table2. *Description of modified 64 – bit binary comparator design.*

Detail	Stage 0^{th}	Stage 1^{st}	Stage 2^{nd}	Transistor Count
Design	Same as Existing	Same as Existing	Same as Existing	1276
Nature of Output	Actual	Inverse	Actual	

Table3. *Simulation data with 5.0 V input and 25°C temperature.*

Design parameter	A<B	A>B	A=B
Existing delay(ns)	1.3ns	1.4ns	1.5ns
Existing power(mw)	517mw	453mw	244mw
Modified delay(ns)	0.9ns	1.1ns	1.2ns
Modified power(mw)	175mw	152mw	45mw
Existing Power delay product(watt-sec)	672ws	634ws	366mw
Modified Power delay product(watt-sec)	157ws	167ws	54ws

6. CONCLUSION

In the modified design at 5v input voltage and 25°C temperature PDP for output "A less than B" (A_LT_B) is decreased by 23%, PDP for output "A greater than B" (A_GT_B) is decreased by 26% and PDP for output "A equal to B" (A_EQ_B) is decreased by 15%. In modified 64 – bit binary comparator design there is a decrease in power consumption, delay and power delay product so modified 64 – bit binary comparator design is used for the better performance applications.

ACKNOWLEDGEMENTS

I am thankful to HOD, Department of ECE for providing necessary permission to carry out this work.

REFERENCES

[1] M. Morris Mano "Digital Design" Pearson Education Asia.3'dEd, 2002

[2] R. Zimmermann and W. Fichtner, "Low Power Logic Styles: CMOS versus Pass Transistor Logic" IEEE Journal of Solid State Circuits, Vo1.32, No.7, pp1079-1 090, July 1 997.

[3] S. Kang and Y. Leblebici "CMOS Digital Integrated Circuit, Analysis and Design" Tata McGraw-Hili, 3m Ed, 2003.

[4] A. Bellaouar and Mohamed I. Elmasry, "Low Power Digital VLSI Design: Circuits and Systems" Kluwer Academic Publishers, 2ndEd, 1 995.

[5] C.-H. Huang and J.-S. Wang, "High-performance and power efficient CMOS comparators," IEEE J. Solid-State Circuits, vol.38, no.2, pp. 254-262, Feb. 2003.

[6] H.-M. Lam and c.-Y. Tsui, "High-performance single clock cycle CMOS comparator," Electron. Lett., vol. 42, no. 2, pp.75-77, Jan. 2006.

[7] H-M. Lam and c.-Y. Tsui, "A MUX-based high performance single cycle CMOS comparator," IEEE Trans. Circuits Syst. II,Exp. Briefs, vol. 54, no. 7, pp.591 -595 July 2007.

[8] Pierce Chuang, David Li, and Manoj Sachdev, Fellow, IEEE "A Low-Power High-Performance Single-Cycle Tree-Based 64-Bit Binary Comparator" IEEE Transactions on Circuits and Systems-II: Express Briefs, Vol. 59, No.2, February 2012.

[9] F. Frustaci, S. Perri, M. Lanuzza, and P. Corsonello, "A new low power high - speed single - clock -cycle binary comparator," in Proc. IEEE Int. Symp. Circuits Syst., pp. 31 7-320, 2010.

[10] S. Perri and P. Corsonello, "Fast low-cost implementation of Single-clock-cycle binary comparator," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 55, no. 12, pp. 1239-1243, Dec. 2008.

[11] Arkadiy Morgenshtein, Alexander Fish, and Israel A. Wagner," Gate-Diffusion Input (GDI): A Power-Efficient Method for Digital Combinatorial Circuits" IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 1 0, No. 5, pp.566-581, October 2002.

[12] Arkadiy Morgenshtein, Student Member, IEEE, Michael Moreinis, and Ran Ginosar, Member, IEEE, "Asynchronous Gate Diffusion-Input (GDI) Circuits" IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 12, No. 8, pp.847-856, August 2004.

AUTHORS' BIOGRAPHY

T.Mounika has completed B.Tech from Talla Padmavathi College of Engineering in 2013 and pursuing M.Tech 2nd year from Vaagdevi College of Engineering.

P.Prasad Rao has currently working as Head of the Department of Electronics and Communication Engineering.