International Journal of Innovative Research in Electronics and Communications (IJIREC)
Volume 2, Issue 3, May 2015, PP 24-31
ISSN 2349-4042 (Print) & ISSN 2349-4050 (Online)
www.arcjournals.org

Design and Analysis for Low Power High Noise Tolerance Circuit

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Abstract: *Digital integrated circuit noise has become one of the foremost issues in the design of very deep submicron VLSI chips. Noise in digital integrated circuits refers to any phenomenon that causes the voltage at a node to deviate from its nominal value. While these noises always existed, in the past they had little impact on the performance of integrated circuits and were often neglected. In this paper we have reduced the noise in deep submicron region. Thus we have to improve the noise tolerance of the dynamic circuits for better performance of the VLSI chips in deep submicron region at low supply voltages where the dynamic circuits are mostly affected by the noise. Thus a proposed a circuit which consume less power and have high noise tolerance.*

1. INTRODUCTION

Dynamic CMOS logic circuits are used in high performance VLSI chips in order to achieve very high system performance. Noise is a major issue in design of dynamic CMOS logic circuits. In deep submicron region noise tolerance of dynamic CMOS logic circuit is very poor and they are more prone to logic failure. Dynamic circuits offer compactness, higher speed as compared to static CMOS circuits. However aggressive scaling of device and interconnect dimensions, power supplies in deep submicron region have further degraded the reliability of dynamic circuits. Noise is digital integrated circuits refers to any phenomenon that causes the voltage at a node to deviate from its nominal value [1]. Compared to static CMOS logic, dynamic logic offers good performance. Wide fan-in dynamic logic such as domino is often used in performance critical paths, to achieve high speeds where static CMOS fails to meet performance objectives. However, domino gates typically consume higher dynamic switching and leakage power and display weaker noise immunity as compared to static CMOS gates[2].

2. EXISITING TECHNIQUES

The latest trend in the VLSI design flow is the merging of digital, analog ,mixed signal or radio frequency circuits onto single chip i.e. System On Chip (SOC).The reduced die area and higher performance of the SOC circuits have instigated this trend. However the digital portion of the SOC, being discrete in nature generates an abundance of noise. This noise must be taken into account when integrating the analog radio frequency portion. Isolation technique can be used to shield the analog and RF portion of the SOC from the noisy digital neighbor. But isolation alone is rarely sufficient to resolve all noise issues. Circuit level techniques must be used to increase the noise immunity of the digital as well as the analog blocks

While it is impractical to include every technique in the literature, in this section we present an overview of some significant techniques. These techniques have been classified into five main categories based on the principle of their operations:

2.1. Using Keeper

The simplest way to enhance the noise tolerance of dynamic CMOS logic gates is to employ a weak transistor, known as keeper, at the dynamic node as shown in Fig. 1.1. The keeper transistor supplies a small amount of current from the power-supply network to the dynamic node of a gate so that the charge stored in the dynamic node is maintained. In the original domino dynamic logic work, the gate of the PMOS keeper Wide fan-in domino circuit are used to design high performance register files, ALU front ends, and priority encoders in content addressable memories. Wide domino logic refers is tied to the ground, as shown in Fig. 1.1. Therefore, the keeper is always on. Later, feedback keepers, illustrated in Fig. 1.4, became more widely used because they eliminate the potential DC power consumption problem using the always-on keeper in the evaluation phase of domino gate. We have also shown its schematic view along with simulation waveform.

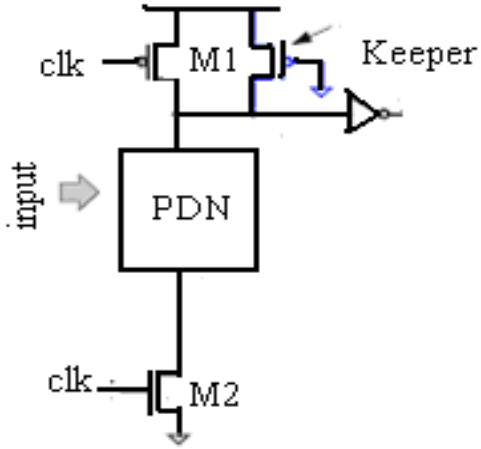


Fig1.1. *Weak-always-on Keeper [4]*

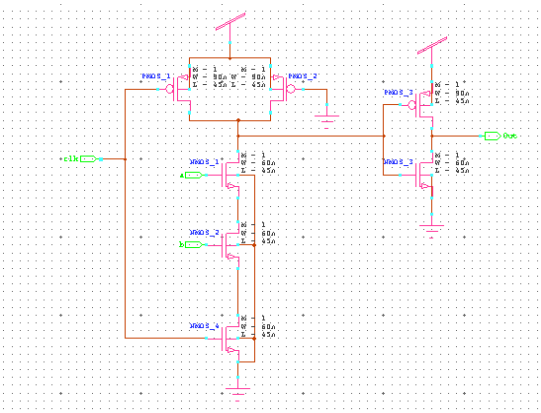


Fig1.2. *Weak-always-on Keeper Schematic*

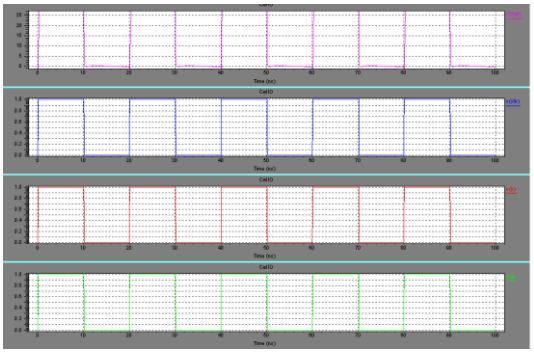


Fig1.3. *Weak-always-on Keeper Simulation Waveform*

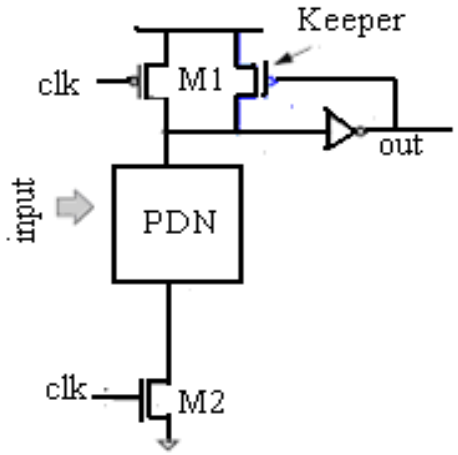


Fig1.4. *Feedback Keeper [4]*

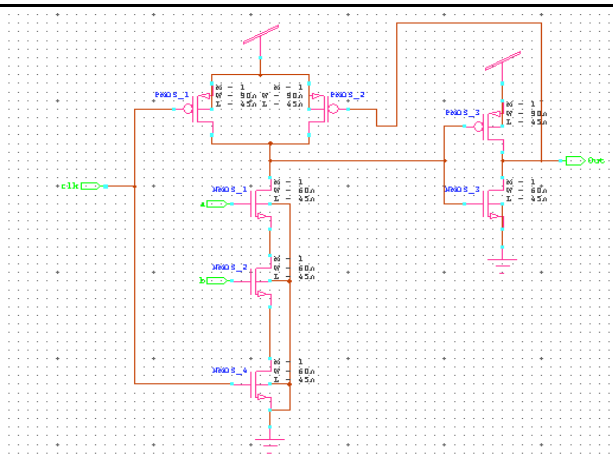


Fig1.5. *Feedback Keeper Schematic*

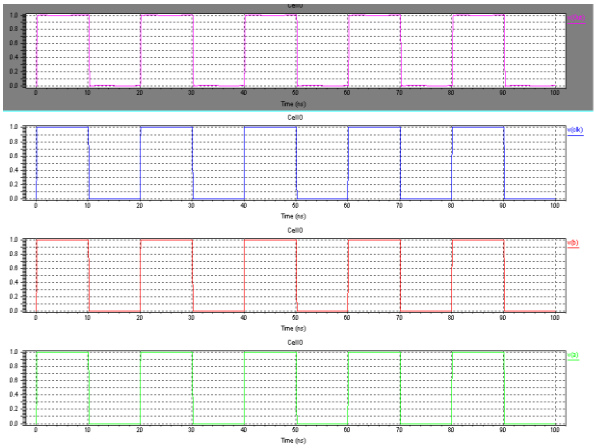


Fig1.6. *Feedback Keeper Simulation Waveform*

2.2. Mirror Technique

Mirror Technique and Twin Transistor Technique are the major techniques based upon this strategy. These techniques are shown in the figures below. Mirror technique requires two identical NMOS evaluation nets. One additional NMOS transistor M1, it's gate voltage is controlled by output signal, provides a conduction path between the common node of evaluation nets and VDD. This technique employs the principle of a Schmitt trigger which can be explained as follows: during the precharge phase, the clock signal Φ turns M2 on, and output voltage Vout is charged to logic high. Assuming that the common node voltage Vx is initially discharged, and then Vx reaches the value VDD-Vtn. Due to body-effect, the switching threshold voltage of the top NMOS net is increased, thereby increasing the noise immunity.

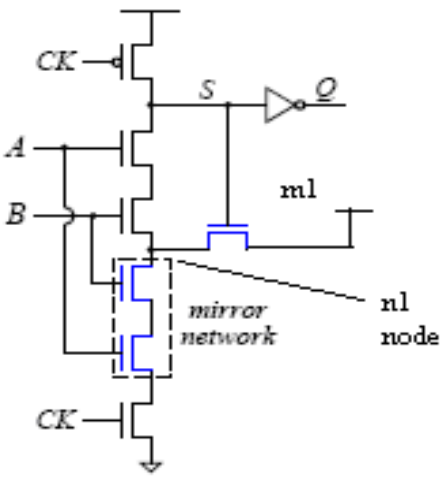


Fig2.1. *Mirror Technique [5]*

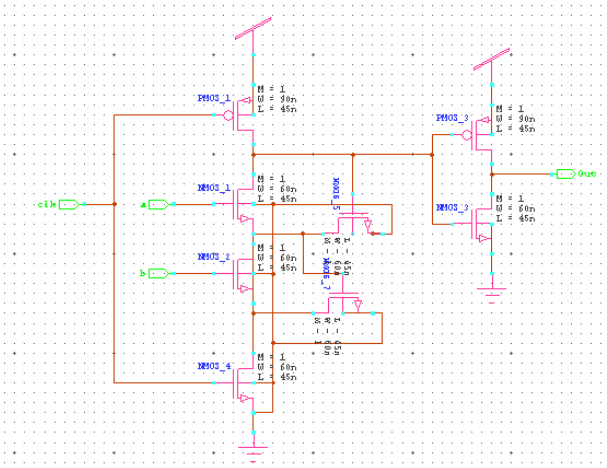


Fig2.2. *Mirror Technique Schematic*

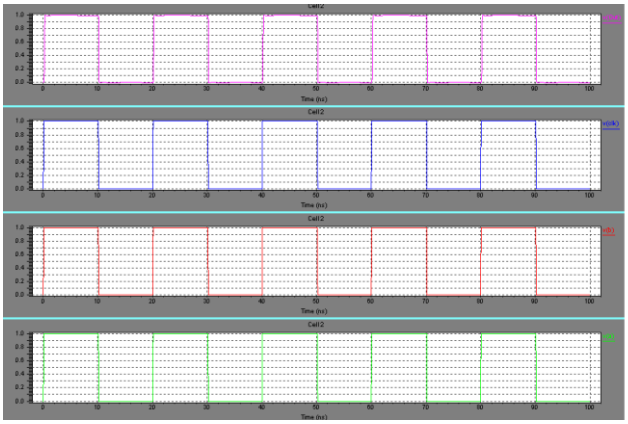


Fig2.2. *Mirror Technique Simulation Waveform*

2.3. Constructing Complementary p-Network

The basic principle of this class of techniques is to construct a weak complementary p-network to prevent the dynamic node from being float in the evaluation phase. One such technique is illustrated in Fig. 3.1. The gate operates in a similar way as a normal domino gate in the precharge phase.

In the evaluation phase, the logic gate behaves as a skewed CMOS logic gate. Therefore, the switching threshold voltage of the dynamic logic gate is equivalent to that of a skewed CMOS logic gate. In additional to the silicon area overhead associated with the pull-up network, a major drawback of this technique in practice is its ineffectiveness in dealing with very wide logic gates, for example, wide OR gates, where dynamic logic styles really outshine static CMOS logic gates in performance.

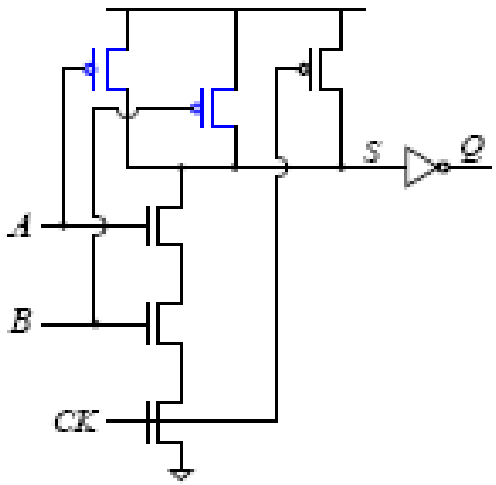


Fig3.1. *Complementary p-network*

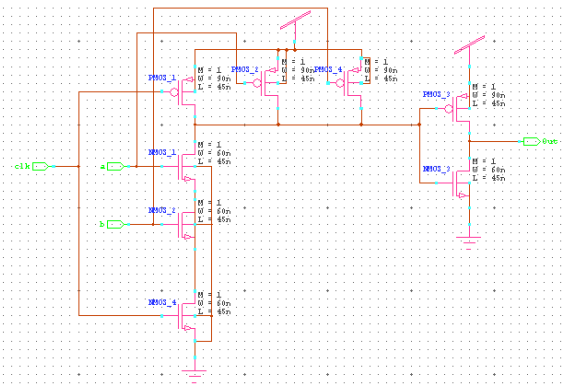


Fig3.2. *Complementary p-network Schematic*

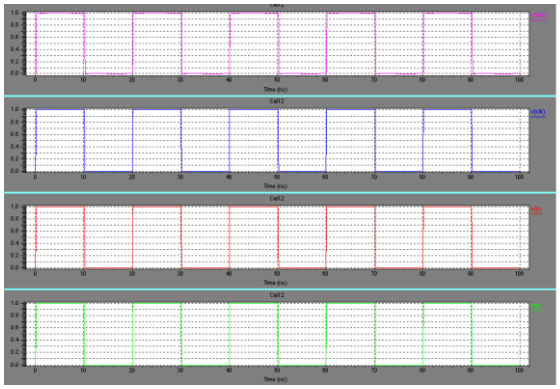


Fig3.3. *Complementary p-network Simulation Waveform*

3. PROPOSED DESIGN

All the above circuits are used for low power but due to the reduced noise immunity of the dynamic logic circuits in deep submicron region our objective is to reduce the noise in deep submicron region. Thus we have to improve the noise tolerance of the dynamic circuits for better performance of the VLSI chips in deep submicron region at low supply voltages where the dynamic circuits are mostly affected by the noise. Thus a proposed a circuit which consume less power and have high noise tolerance.

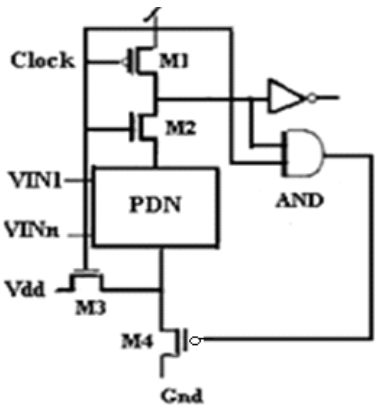


Fig4.1. *High Performance Noise Tolerant design*

It consists of 7 parts:

- Transistor M1 is the precharging transistor.
- Transistor M2 is used as a stacking transistor.
- Transistor M3 is used as source potential raising transistor.
- Transistor M4 is used as conditionally clocked discharging transistor
- Pull-Down Network Defines the logical functionality of the circuit.
- AND gate has been built using pass transistor logic.

Inverter is used for providing Domino functionality.

Schematic view of proposed design is as shown in Figure 4.2.

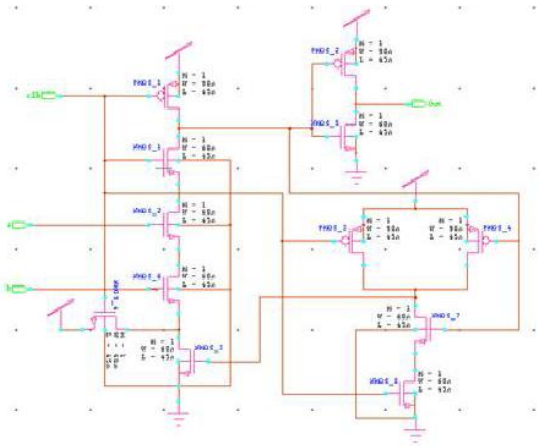


Fig4.2. *Schematic View of High Performance Noise Tolerant design*

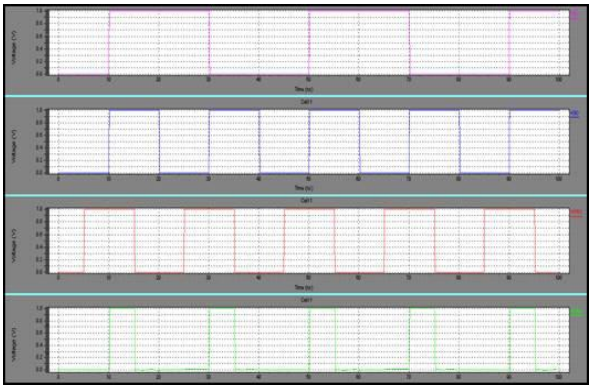
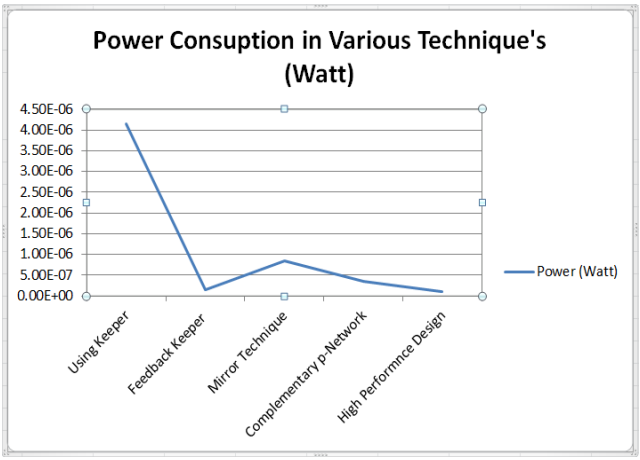


Fig4.2. *Simulation results of High Performance Noise Tolerant design*

4. RESULTS

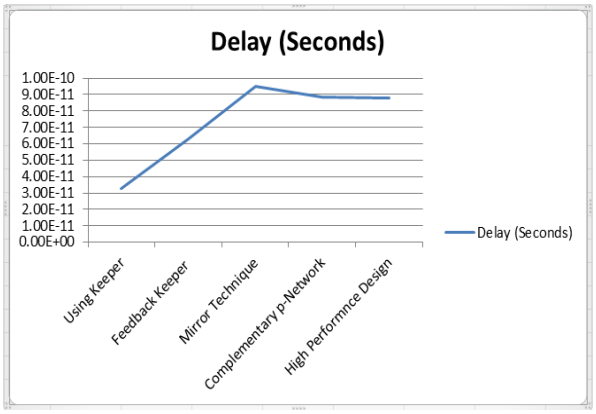
We have reviewed the simulation results from various techniques, and found that the results obtained through our proposed design, was more accurate and fulfilling the criteria of high performance dynamic CMOS logic design. We have minimized the power consumption up to great extent, Due to presence of the NAND gate, in precharging state the entire lower half pulldown network is in off state, that is saving a lot of power and we have selected source transistor in such way that in evaluation state the voltage level at the output can be maintained as in precharge state. So the deviation of output voltage level can be fixed that is the basic requirement for noise tolerant design. Here I am providing the power and delay results obtained through the simulation of various design, and product.



Graph4.1. *Power Consumption Result's*

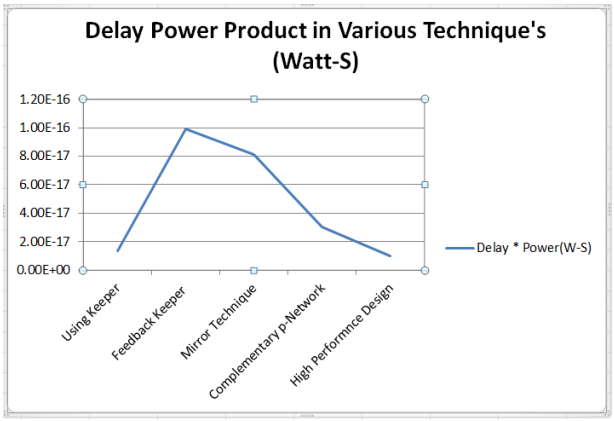
Here we have compared the power consumption in for various techniques, and it is clear that we are saving a lot of power using our design.

Below graph is shown for delay analysis in various techniques, and we can say that our design is not taking more time in input output response. This is major breakthrough in electronic industries, our circuits will helpful for designing of highly complex logic with less power consumption and delay. We have used the tanner 14.1 to implement this design and simulation waveform.



Graph4.2. *Delay Analysis in Different Design*

Following is provided for the delay power product.



Graph4.2. *Delay Power product in Different Design*

5. CONCLUSION

Effective noise-tolerant design techniques are vital to the success of VLSI circuits as noises become an ever-increasing problem with the relentless scaling of process technology. A desirable noise-tolerant technique should be able to improve circuit robustness against all noise types, be suitable for all logic functions, and have very low overhead in silicon area, circuit speed, and power consumption. In this paper, such a noise-tolerant design technique is proposed.

REFERENCES

[1] Umesh Dutta, Pankaj Kumar, Naresh Kumar "Noise Tolerance Enhancement with Leakage Current Reduction in Dynamic Logic Circuits" International Journal of Scientific Engineering and Technology, Volume No.1, Issue No.3, pg : 137-142, 01 July 2012.

[2] Dr.T.Jayachandra Prasad, C.Sreelakshmi, "Noise-Tolerant CMOS Domino VLSI Circuits in VDSM Technology" International Journal of Advanced Computer Science and Applications, Vol. 2, No. 4, 2011.

[3] Ajay Kumar Dadoria, Uday Panwar, "Comparison on Different Domino Logic Design for High Performance and Leakage-Tolerant Wide OR Gate" Int. Journal of Engineering Research and Applications, ISSN : 2248-9622, Vol. 3, Issue 6, Nov-Dec 2013, pp.2048-2052.

[4] Walid Elgharbawy, Pradeep Golconda, and Magdy Bayoumi " Noise-tolerant high fan-in dynamic CMOS circuit design" in GLS VLSI'05, Chicago,USA, April 17–19, 2005.

[5] Mendoza-Hernandez, F. Linares, M.Champac, V.H. "An improved technique to increase noise-tolerance in dynamic digital circuits" Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium page(s): II- 489-92 vol.2 May 2004.

[6] Frustaci, F.; Dept. of Electron., Univ. of Calabria, Rende; Corsonello, P.; Perri, S.; Cocorullo, G," High-performance noise-tolerant circuit techniques for CMOS dynamic logic" Circuits, Devices Systems, IET (Volume:2 , Issue: 6) December 2008 p.p. 537 – 548.

[7] Kumar Yelamarthi, and Chien-In Henry Chen, " Timing Optimization and Noise Tolerance for Dynamic CMOS Susceptible to Process Variations" IEEE transactions on semiconductor manufacturing, vol. 25, no. 2, may 2012 p.p. 255-265.

[8] Pierce Chuang, David Li, and Manoj Sachdev, "Design of a 64-Bit Low-Energy High-Performance Adder using Dynamic Feed through Logic", Proc. of IEEE International Symposium on Circuits and Systems, 2009, pp. 3038-3041.

[9] Pierce Chuang, David Li, and Manoj Sachdev, "Constant Delay Logic Style" IEEE transactions on very large scale integration (VLSI) systems, vol. 21, no. 3, March 2013 p.p.554-565.

[10] Mazumdar, K.,Pattanaik, M, " Noise tolerance enhancement in low voltage dynamic circuits" Design Technology of Integrated Systems in Nano scale Era, 2009. DTIS '09. 4th International Conference on 6-9 April 2009 p.p. 23 – 27.

[11] Yelamarthi, K., Chen, C.-I.H," Timing Optimization and Noise Tolerance for Dynamic CMOS Susceptible to Process Variations" Electronics, Computing and Communication Technologies (IEEE CONECCT), 2014 IEEE International Conference on 6-7 Jan. 2014 p.p.1-5.

[12] Fabio Frustaci, Pasquale Corsonello, Stefania Perri, and Giuseppe Cocorullo "High-performance noise- tolerant circuit techniques for CMOS dynamic logic", Proc. IET Circuits Devices Syst., 2008, Vol. 2, No. 6, pp. 537–548.