

Low Power High Speed Voltage Level Shifter for Sub-Threshold Operations

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Abstract: *We present ultra low power application, low power supply(vdd) of sub-threshold logic results in significant power reduction. The large supply voltage difference b/w sub-threshold core logic & i/o makes extremely challenging to convert signals from core circuit to i/o circuit in this we propose a level converter like static and dynamic level converters for sub-threshold logic high voltage clock signals needs to be delivered through separate clock path from core logic, leading clock synchronization problem b/w high voltage and low voltage clocks to overcome this issue we employed clock synchronizer.*

Index Terms: *Level converter, subthreshold logic, subthreshold operation, ultra-low voltage operation.*

1. INTRODUCTION

The demand for low power circuit design has increased significantly due to the explosive growth of battery operated portable applications like laptop computers and cellular phones. In order to reduce power consumption, several techniques such as voltage scaling [1] and switching activity reduction [2] are widely used. However, these methods still fail to deliver ultra-low requirements of some portable applications such as wireless sensor networks and implantable medical devices. To cope with this, researchers have explored the possibility of digital sub-threshold logic [3]–[5]. Since ultra-low supply voltage (VDD) is used in sub threshold logic, we can obtain significant power savings. Moreover, low gate capacitance in weak inversion [6] leads to more switching power reduction. The ultra-low core VDD, however, results in many design challenges as well. For example, due to vast difference between core VDD and high input/output (I/O) supply voltage (VDDH), it is difficult to convert signal from core logic to I/O circuits. To achieve good drive current for large impedance load and high immunity to noise signals, I/O circuits employ higher supply voltage than that of the core logic. Hence, level converters are required for efficient conversion of I/O signals between two voltage domains. Unfortunately, conventional level converters, designed to convert low super threshold input to high super threshold output, are not effective to convert sub threshold input to super threshold voltage output. Static level converters, shown in Fig. 1(a) and (b), fail such conversion due to extremely small pull-down current of low voltage domain compared to pull-up current of high voltage domain.

For a dynamic level converter [see Fig. 1(c)], the combat between pull-up and pull-down is not a critical issue since pull-up devices are turned off during evaluation phase. Nonetheless, it is still difficult to apply conventional dynamic level converters. In this work, we design a level converter based on dynamic logic style for sub threshold logic

[10]. Here, we assume that high voltage clock is delivered to I/O circuits through the separate clock path from core logic. To synchronize the high voltage clock signal with the sub threshold voltage clock signal, we propose a *Clock Synchronizer*. The *Clock Synchronizer* employs domino logic style, prone to leakage noise at slow speed of sub threshold operation. To improve noise margin of the *Clock Synchronizer*, we propose a new keeper technique using a *Reduced Swing Inverter*. We fabricated a test chip in 130-nm CMOS to verify the proposed techniques. The test chip measurement results show that the proposed dynamic level converter successfully converts the input voltage as low as 0.1V to the high output voltage (2.5 V).

2. CONVENTIONAL LEVEL CONVERTERS

There are different types of level converters have been proposed in previously reported literature[7]-[9].fig1&2 are static level converters and fig3 is a dynamic level converter, in fig1 dcvsl(differential cascade voltage switch logic) level converter MN1 is the i/p. if we give i/p as '1' then MN1 becomes ON then data goes to GND. So, we get o/p B as '0'. Then '0' is the i/p to MP2.transistors then MP2 will be ON, then OUT is '1'.then OUT1 becomes i/p to the MP1 transistor then it becomes off. So, charging and discharging takes place from fig2 here VDDL is the i/p to the ckt then Nmos transistor will be off mode, then the o/p becomes '0'then '0' becomes i/p to the cmos. Then pull up becomes ON and pull down becomes OFF then the o/p is '1'.this acts as i/p to the feedback pmos transistor then it becomes OFF. So, o/p is '0'. Again '0' is the i/p to cmos this process continuous. So, here charging and discharging takes place. In FIG c dynamic level converter depends upon clock. If clk is '1' (evaluation mode), clock is '0' (precharge mode).

If clock is '1'.IN is the i/p, if we give IN as '1' then it becomes ON then VDDH becomes short circuit, and then OUT become '1'. The o/p '1' becomes i/p to the feedback pmos then pmos becomes OFF this

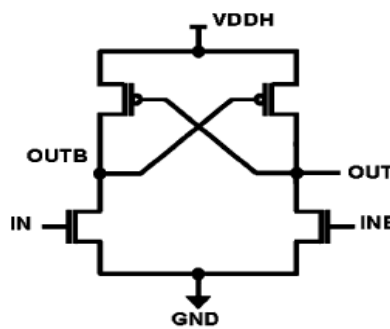


Fig 1. DCVSL level converter

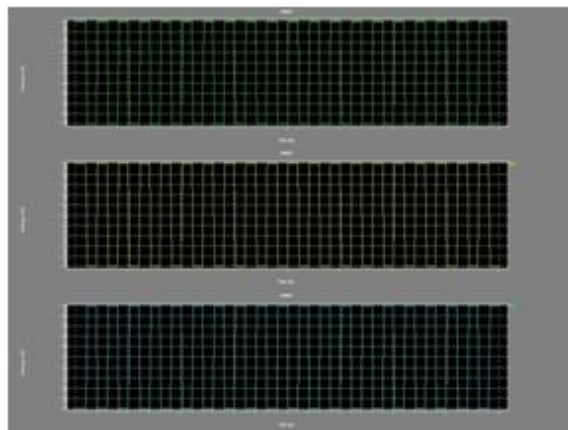


Fig 2. Simulation result of DCVSL level converter

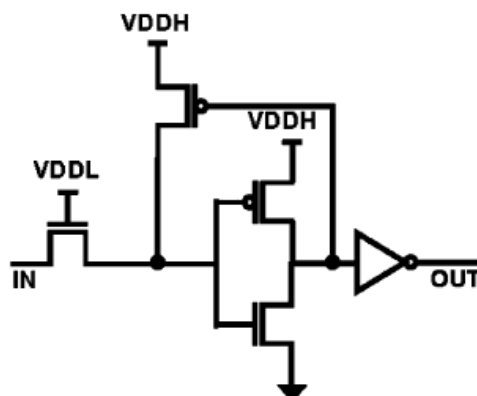


Fig 3. Pass transistor half latch based level converter

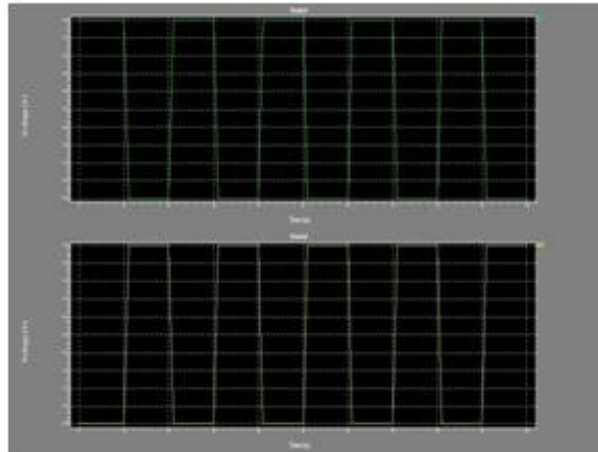


Fig 4. Simulation result of Pass transistor half latch based level converter

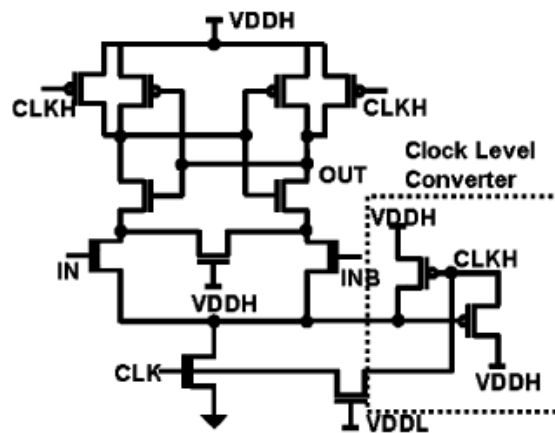


Fig 5. Dynamic level converter

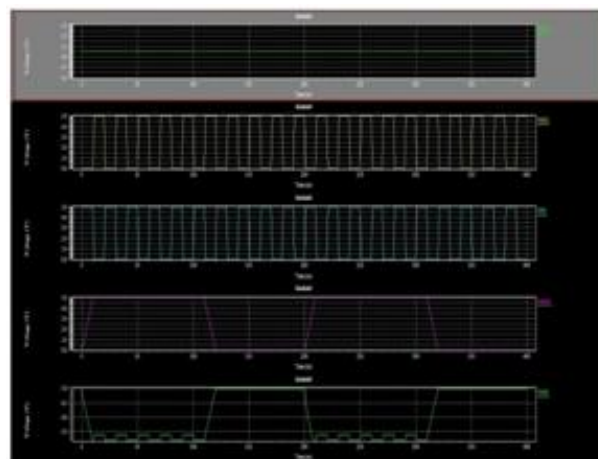


Fig 6. Simulation result of Dynamic level converter

process continuous. Here we are using clock level converter the main purpose of this is what ever clock we give it converts s high. Here we are giving clock H. If we give clk='0' then VDDL='0'then VDDH (CLKH) becomes ON, then o/p is '1'.then '1' is the i/p to VDD Pmos then it becomes OFF. Then VDDH means to min i/p it gives 5V o/p.

If we give clock as '1' then VDDL ON it becomes i/p to CLKH. The CLKH becomes OFF then o/p is '0'.It acts as i/p to VDDH Pmos becomes ON it gives o/p as high CLK'1'.

3. PROPOSED DYNAMIC LEVEL CONVERTER FOR SUB-THRESHOLD LOGIC

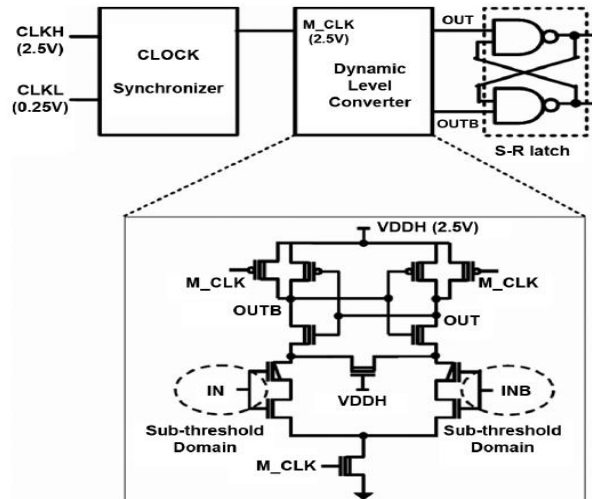
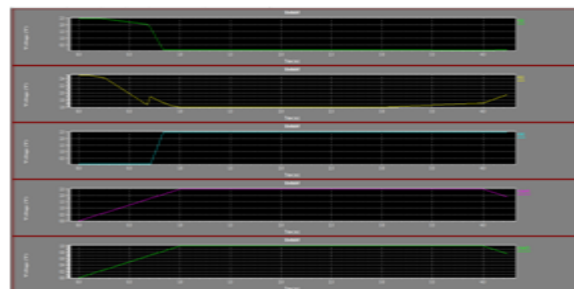


Fig proposed Dynamic Level converter

Above circuit is connected in the form of feedback N/W because it acts as a memory if we want to save data that can be connected in feedback form. In CLK pulse it stores data until next clock pulse arises. In schematic clock synchronizer circuit[11] here we are given VDD as 2.5V & CLKH Is the i/p. SO, Pmos will be in OFF mode then M1 will be ON, then o/p is '0'. M-CLK o/p nothing but '1'. Here even though if we are giving CLK'L to the Nmos i.e. M3&M2 this is called sub-threshold domain. It means we are giving sub-threshold voltage to the M3&M2 then both Nmos transistors will be in OFF mode. instead of CLKH, M-CLK is taken as a dynamic level converter, if transistor gate length increases then leakage current increases. CLK fails due to the weak pull down strength of the Nmos transistors operating in a sub-threshold region compared to the keeper Pmos working in a sub-threshold region the main function of this is when ever CLKH&CLKL is '1' then o/p will be '1'.

We proposed a new keeper design is reduced swing inverter [11]. If we gives i/p as '0' then MP3 will be ON and node 'OUT' is charged to VDDH as '1'. If we give i/p as '1' then both MP2&MP3 are OFF mode.



So, node OUT is disconnected to GND. this node is not completely discharged. Charge distribution takes place b/w node OUT and capacitor 'C1'. This leads to "reduced o/p voltage swing". i.e.

- Here no direct ON current path like conventional inverter.
- Static power consumption can be avoided.
- Leakage noise may destroy the voltage at node 'OUT'. In order to prevent the node from losing its charge, we add two diodes like MP1&MP2.
- If "OUT" goes a below certain potential the diodes will be ON then node 'OUT' start to recharge, due to diode voltage drop the o/p potential cannot rise beyond a certain point. So, 'OUT' node can be preserved constantly while i/p is logic '1'. by using this method we can decrease voltage.

In reduced swing inverter[11] CLKH is the i/p to the Pmos, then Pmos will be OFF then its o/p is given is given to the i/p of the inverter then the o/p is '1'. again the o/p is given to the i/p of another inverter then the o/p is '0'. so, '0' is the i/p to the reduced swing inverter then its o/p will be

'1'.then MP1 will becomes OFF then 'OUT' will be '0' this process repeats. By combining clock synchronizer & reduced swing inverter it reduces the noise that occurs in clock synchronizer by this we can reduce noise

Schematic of Clock Synchronizer

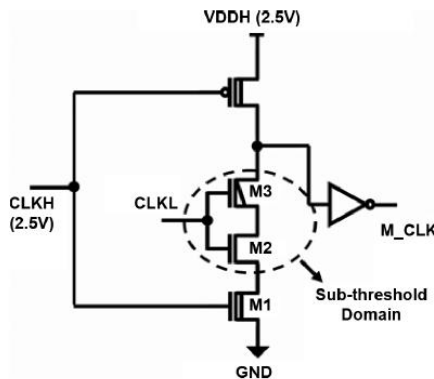
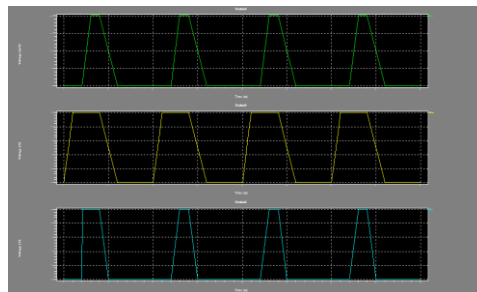


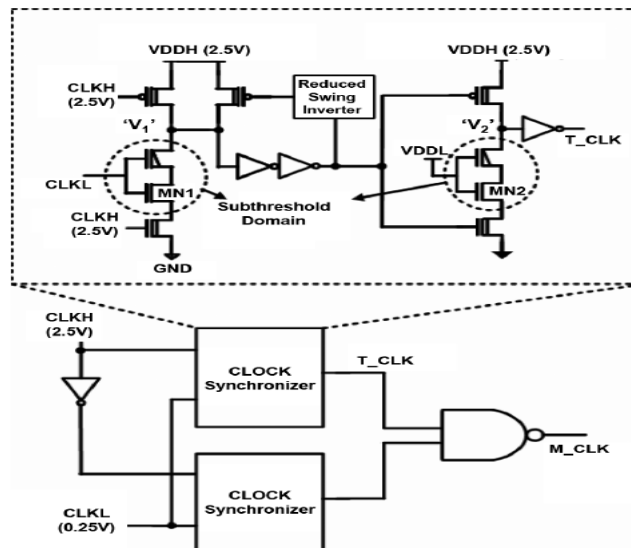
Fig Clock Synchronizer

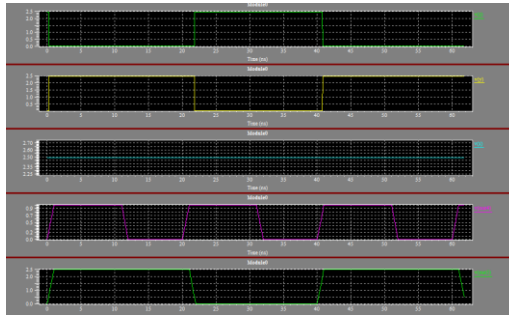
In clock synchronizer circuit we are giving vdd as 2.5 V and CLK-H as the input. So, pmos will be OFF mode. The M1 will be ON. Then output is '0'. M-CLK output nothing but '1'. Here, even though if we give CLK 'L' to the Nmos i.e. M3 & M2 then this is called subthreshold domain, it means we are giving subthreshold voltage to the M3 & M2 then both Nmos transistors will be in OFF mode.



Instead of CLK H, M-CLK is taken as a dynamic level convertor, if transistors gate length increases then leakage current will be increased. CLK fails due to weak pull down strength of the Nmos transistor operating in a subthreshold region compared to keeper Pmos working in a subthreshold region. The main function of the clock synchronizer is whenever CLK 'H' and CLK 'L' is '1' (in evolution mode) then output will be '1'.

4. FINAL ARCHITECTURE OF THE CLOCK SYNCHRONIZER

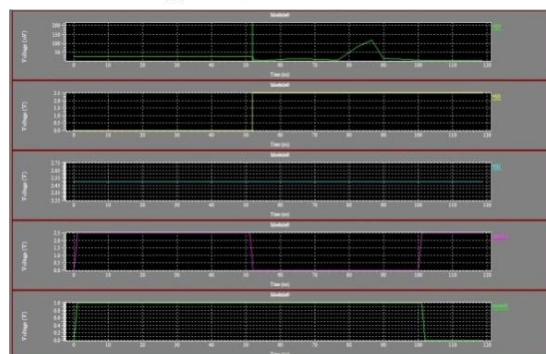
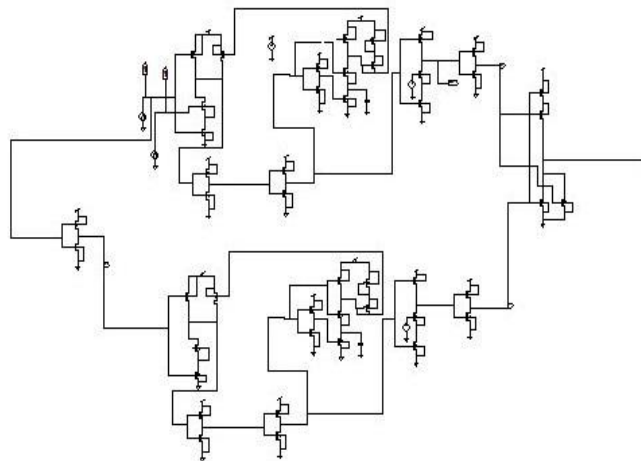




In duplicated clock synchronizer we are using two complementary precharge signals CLKH&CLKL. One of the two clock synchronizer is evaluated at the rising edge of CLKL. Making M-CLK signal synchronized with the rising CLKL making M-CLK signal synchronized with the rising CLKL regardless of skew b/w CLKH&CLKL. It works as whenever CLKH&CLKL will be HIGH. i.e. '1' the o/p will be HIGH, when the evaluation at the rising edge. Here dead zone occurs when the falling delay of the clock synchronizer is much smaller than its rising delay.

In final architecture of the clock synchronizer here CLKH is the i/p to the Pmos then V1 will be '0'. This is the i/p to the inverter then we get o/p of the 2nd inverter is '0'. Then it becomes i/p to the reduced swing inverter then o/p will be '1'. It is the i/p to the Pmos then o/p is '0'. this process repeats at OUT1. we will get constant o/p as '0'. Because here we get o/p as 0.48mv i.e. less than '1'. It always considered as '0'. Then T-CLK will be '1'. The main functionality of this is dead zones occurring in the duplicated clock synchronizer will be eliminated in the final architecture of the clock synchronizer.

5. FUTURE SCOPE



In final architecture of the clock synchronizer, here we are replacing NOR Gate in place of NAND Gate, when CLKH is the i/p to the Pmos then V1 will be '0'. This is the i/p to the inverter then we get o/p of the 2nd inverter is '0'. Then it becomes i/p to the reduced swing inverter then o/p will be '1'. It is the i/p to the Pmos then o/p is '0'. this process repeats at OUT1. we will get constant o/p as '0'. Because here we get o/p as 0.48mv i.e. less than '1'. It always considered as '0' Then T-CLK will be '1'. The main functionality of this is dead zones occurring in the duplicated clock

synchronizer will be eliminated in the final architecture of the clock synchronizer. The main advantage by using NOR Gate is, by comparing to NAND and NOR Gate, in NOR Gate more power consumption decreases.

6. CONCLUSION

With ultra-low power supply voltage, digital sub-threshold logic can reduce power consumption significantly. However, vast difference between the high I/O voltage and the low core supply voltage makes the level conversion extremely difficult. Conventional static level converters fail to convert ultra-low voltage signal of sub-threshold logic to high voltage of I/O circuit even with voltage doubling [10] and pull down device stacked with zero Nmos [11]. Although conventional dynamic level converter can convert ultra-low voltage signal, clock synchronization between low voltage clock and high voltage clock impedes its application for sub-threshold logic. In this work, we proposed a novel *Clock Synchronizer*. From high voltage clock (CLKH) and ultra-low voltage clock (CLKL) delivered through separated clock paths, the *Clock Synchronizer* generates new high voltage clock signal (M_CLK) synchronized with CLKL. In addition, we designed a novel keeper using *Reduced Swing Inverter* to improve noise margin of the *Clock Synchronizer*. Since the *Reduced Swing Inverter* makes the keeper operate at near-threshold region, we can obtain proper keeper strength matched with sub-threshold evaluation current using conventional sizing techniques.

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