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Designing Nano Scale CMOS Adaptive PLL to Deal, Process Variability and Leakage Current for Better Circuit Performance

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Abstract: *The performance of the CMOS circuit decreases with the variability and leakage current. To accommodate this issue in Adaptive Phase Lock Loop (PLL), a self-healing prescaler, a self-healing voltage-controlled oscillator (VCO), and a calibrated charge pump (CP) are presented. The main reason for changes in variability and leakage current is temperature that operates in 100^0 C. The undesired leakage currents degrade the accuracy and resolution of analog circuits and make digital dynamic circuits not to work properly. This self-healing prescaler and self-healing voltage-controlled oscillator detect the leakage current itself and compensate that leakage current automatically. To implement this technology used is in nano scale that is used here is 180nm.*

Keywords: *PLL, Self-healing VCO, Self-healing prescaler, leakage current.*

1. INTRODUCTION

As the technology grows to nanometer scale the performance of the device decreases due to change in the variability and leakage current. The process variability causes degradation in the mismatch and performance of the device which are designed in nanometer scale. The leakage current produce in the device due to the device design and the leakage current produce due to high temperature which that device is in that working environment this cause degradation in the accuracy and resolution of the analog circuits and make not to work properly in the digital circuits. As now a day's all device are turning to digitalization the correct performance of the device is required mainly in the successful of that technology. This leakage current grows very fast in the high temperature.

This is the issue existed in nano technology. To recover this issue the device taken here is a Phase Lock Loop.

The Phase Lock Loop has a wide verity of application in this modern era especially in wired and wireless communication system. Some of the applications of the PLL are in modulation and demodulation, frequency synthesizers, clock and data recovery and in telecommunications. The device mismatch and leakage current cause the common-mode voltage of the voltage-control oscillator to vary over a wide range frequency. This limits the oscillation frequency and cause the VCO not to oscillate in the worst conditions. Here the Adaptive PLL means the divider circuits which come after the VCO should operate between the highest and lowest frequency.

The widely used divider circuit in PLL is True-Single-Phase-Clocking (TSPC). This TSPC prescaler should work over a wide frequency range to cover the process and temperature variations. For a TSPC prescaler, the undesired leakage currents may limit its frequency range or alter the original states of the floating nodes to have a malfunction. The leakage current and current mismatch in a charge pump (CP) will degrade the reference spur and jitter significantly.

To overcome the above problem a self-healing divide-by-4/5 prescaler and a self-healing VCO are designed in this project

2. CIRCUIT DESCRIPTION

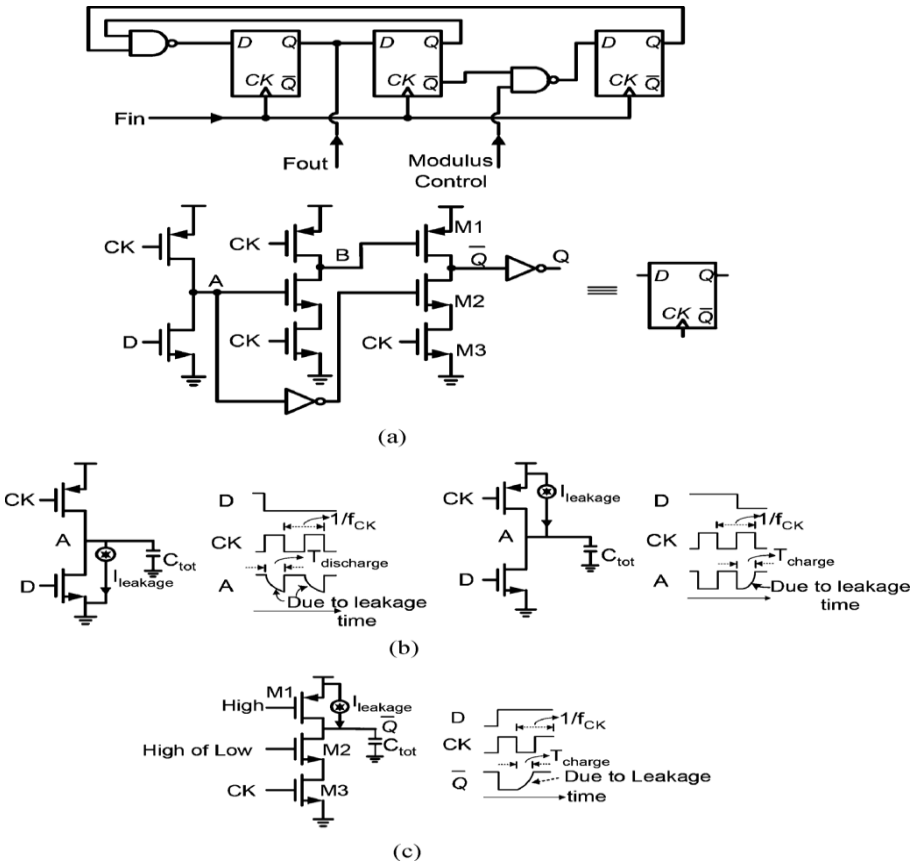

Fig1. (a) *Conventional divide-by4/5 dual-modulus prescaler using TSPC DFFs.* **(b)** *Two kinds of malfunctions occurred at A.* **(c)** *The malfunction occurred at Qbar.*

2.1. Self-Healing Divide-by-4/5 Dual-Modulus Prescaler

The Fig.1 shows conventional divide-by-4/5 dual-modulus prescaler using TSPC DFF's. The undesired leakage current may charge or discharge to alter the states of the nodes A, B, and Qbar in this TSPC DFF as shown in Fig. 1(a).

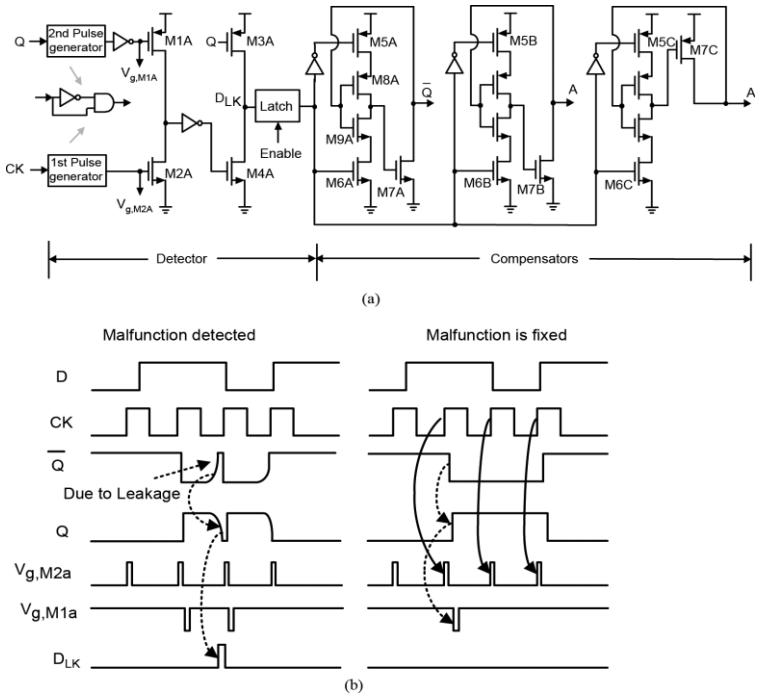

Fig2. (a) *Self-healing circuit and* **(b)** *timing diagrams of a TPSC DFF with and without a malfunction by using a self-healing circuit.*

For example, two kinds of the malfunctions may occur at the node A as shown in Fig. 1(b), respectively. The first case is that the initial state of the node A is high; however, a leakage current discharges it to ground. The second one is that the initial state of the node A is low, but a leakage current charges it to high. To consider the node B in Fig. 1(a), assume that the leakage current charges the node B to be high when CK is high. It will not affect the original state of the node. Thus, the leakage problem occurred at the node B is not considered here. For a malfunction occurred at the node Qbar, the simplified circuit is shown in Fig. 1(c). Assume the transistor M1 is turned off, CK is low, and the initial state of the node is low. Since the node is floating, the leakage current from M1 may charge the node to high and a malfunction occurs. Note that the leakage current through M2 and M3 is smaller than that from M1. It is because the cascode transistors, M2 and M3, induce a lower leakage current.

For example, two kinds of the malfunctions may occur at the node A as shown in Fig. 1(b), respectively. The first case is that the initial state of the node A is high; however, a leakage current discharges it to ground. The second one is that the initial state of the node A is low, but a leakage current charges it to high. To consider the node B in Fig. 1(a), assume that the leakage current charges the node B to be high when CK is high. It will not affect the original state of the node. Thus, the leakage problem occurred at the node B is not considered here. For a malfunction occurred at the node Qbar, the simplified circuit is shown in Fig. 1(c). Assume the transistor M1 is turned off, CK is low, and the initial state of the node is low. Since the node is floating, the leakage current from M1 may charge the node to high and a malfunction occurs. Note that the leakage current through M2 and M3 is smaller than that from M1. It is because the cascode transistors, M2 and M3, induce a lower leakage current.

To detect and heal the above issues occurred at the nodes A and, the proposed self-healing circuit is shown in Fig. 2(a).

This self-healing circuit consists of a detector and three compensators. By using a self-healing circuit, the timing diagrams of a TPSC DFF with and without a malfunction are shown Fig. 2(b), respectively. Assume the signal Enable in the self-healing circuit is low to disable the latch in Fig. 2(a). For a case that the malfunction is detected, the timing diagram is shown in the left side of Fig. 3(b). When the clock CK goes high, the 1st pulse generator outputs a short pulse at the gate of M2A, which goes high to clear D_{LK}. When the input D of the DFF is high, the rising edge of the clock CK triggers the DFF's output Q to go high (or goes low) to turn off M3A.

The 2nd pulse generator outputs a low pulse at the gate of M1A to turn off M4A. Before the next rising edge of CK arrives, Qbar is assumed to be charged to high due to the undesired leakage current. In the meantime, Q goes low to turn on M3A and enables D_{Lk} =1. It indicates that the malfunction of this TSPC DFF occurs. The size ratio of M4A and M3A is 5 to ensure D_{Lk} =0 , when both M3A and

M4A are turned on. It has been simulated and verified for all corners and a supply voltage variation of 10% and the temperature of 0^0 C~100^0 C. For a case that the malfunction is fixed, the timing diagram is shown in the right-hand side of Fig. 2(b) where D_{LK} is always low. In Fig. 2(a), when the signal Enable is high and the malfunction is detected D_{Lk} =1, is latched by a latch and the compensator is active. For example assume the initial state of Qbar is low and the leakage current is charging the node Qbar. Since Qbar is low and D_{Lk} =1, the transistors, M5A–M8A, in a compensator will be turned on. A minimum-sized transistor M7A is used to counteract the leakage current and repair the state of the node Qbar to be low finally. The leakage current is much smaller than that a minimum-size MOS can provide. These circuits have been simulated and verified for all corners and a supply voltage variation of 10% at the temperature of 0^0 C~100^0 C. Similarly, when a malfunction is detected, the compensators will turn on M7B or M7C to counteract the leakage current and repair the state at the node A.

2.2. Self-Healing VCO

A self-healing VCO is realized by four gain stages, a bottom level detector, and a current compensator. Fig. 3(a) shows a bottom-level detector, a current compensator, and a gain stage. This gain stage consists of a differential amplifier with active loads and a cross-coupled pair with digitally-controlled current sources. In the differential amplifier, the transistors, M_1 and M_2 realize

the input stage, and the transistors, M_3 and M_4 act as a variable resistor controlled by Vctrl. The cross-coupled pair, M_5 and M_6, enhances the output swing of this VCO. The output common-mode voltage and the output swing of the VCO are altered by the leakage currents, the total tail currents, and the resistances of M_3 and M_4 They are dependent upon the process variations. For example, when the resistances of M_3 and M_4 are decreased, the oscillation frequency of this VCO is increased. It will result in the output swing decreased and the bottom level is increased. It also leads to a limited oscillation frequency range. If a larger biasing current and the cross-coupled pair with larger dimensions are selected for this VCO, the output swing can be increased. However, it may waste the power when the operation frequency of this PLL is low. In this work, the self-healing VCO using a bottom-level detector can achieve a wide tuning range and low power.

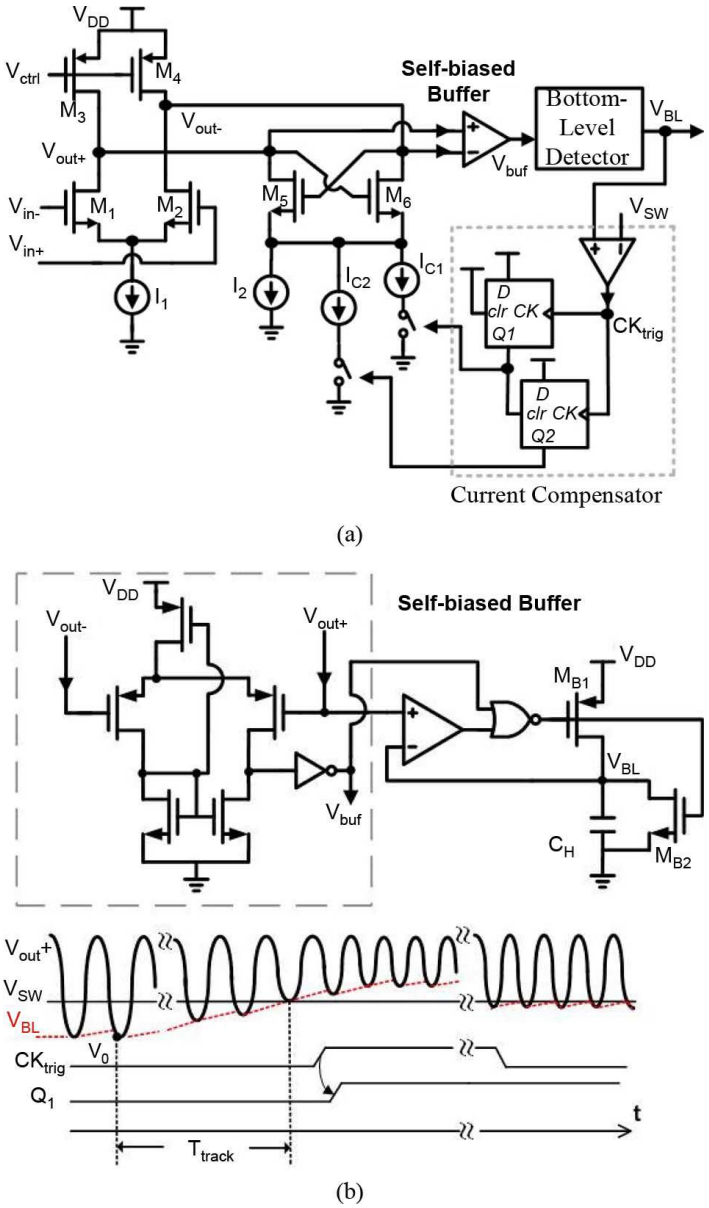

Fig3.(a) *Gain stage, a bottom-level detector, and a current compensator, and* **(b)** *The bottom-level detector.*

The bottom-level detector is shown in Fig. 3(b) and it detects the bottom level of the VCO's output swing. A self-biased buffer enlarges the output of a VCO into a rail-to-rail swing. So, the output, Vbuf, of this self-biased buffer and Vout+ have the same polarity. When Vout+ goes high and Vbuf is high, the NOR gate will enable M_{B1} and disable M_{B2} respectively. The current of the transistor M_{B1} will charge the capacitor, C_H to increase $V_{BL.}$

When Vout+ goes low and Vbuf is low, two cases will be discussed. In Fig. 3(b), if the bottom level of Vout+ is larger than V_{BL} the comparator's output goes high and the NOR gate goes low to enable M_{B1} and disable M_{B2} respectively. The transistor M_{B1} will charge the capacitor, $C_{H,}$ to increase $V_{BL.}$ For the other case, if the bottom level of Vout+ is lower than $V_{BL,}$ the comparator's output goes low and the NOR gate goes high to disable M_{B1} and enable M_{B2} respectively. The transistor M_{B2} will discharge the capacitor, C_H to decrease $V_{BL.}$ In the steady state, the voltage V_{BL} on the capacitor, C_H , will track the bottom level of the VCO's swing. For the current compensator in Fig. 3(a), a reference voltage V_{SW} represents the target bottom level of the VCO's swing and it is compared with V_{BL} by a comparator. When the VCO's bottom level is smaller than the target one or the output common-mode voltage of this VCO is high enough, V_{BL} is larger than V_{SW} Then, the output of the comparator CKtrig goes high and enables Q1. The current compensator enables the auxiliary tail current I_{C1} to lower the output common-mode voltage. The timing diagram is shown in Fig. 3(b). Then, it reduces the VCO's bottom level to be lower Than V_{SW}. If the above case is not true, Q2 will be enabled and turn on the auxiliary tail current I_{C2} It further lowers the VCO's bottom level.

2.3. Phase-Locked Loop

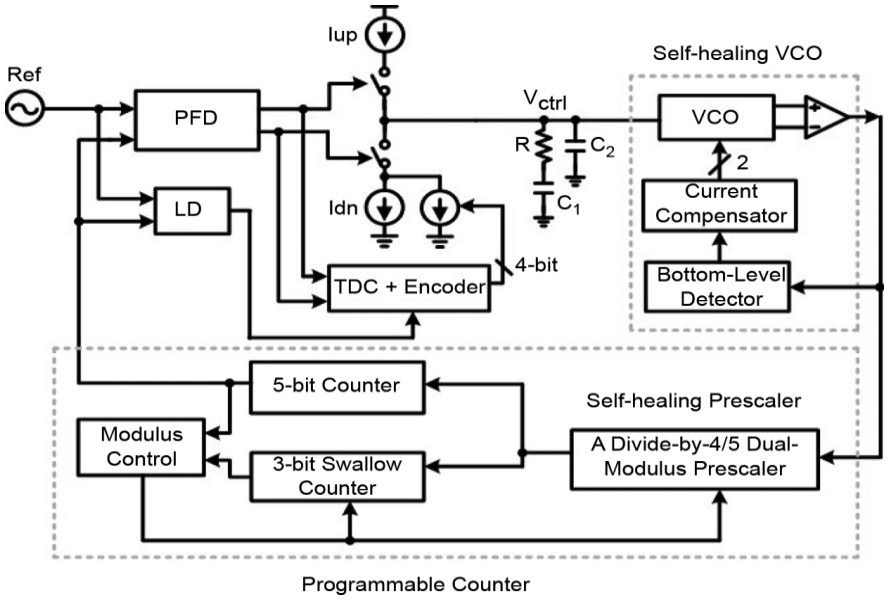

Fig4. *Proposed PLL.*

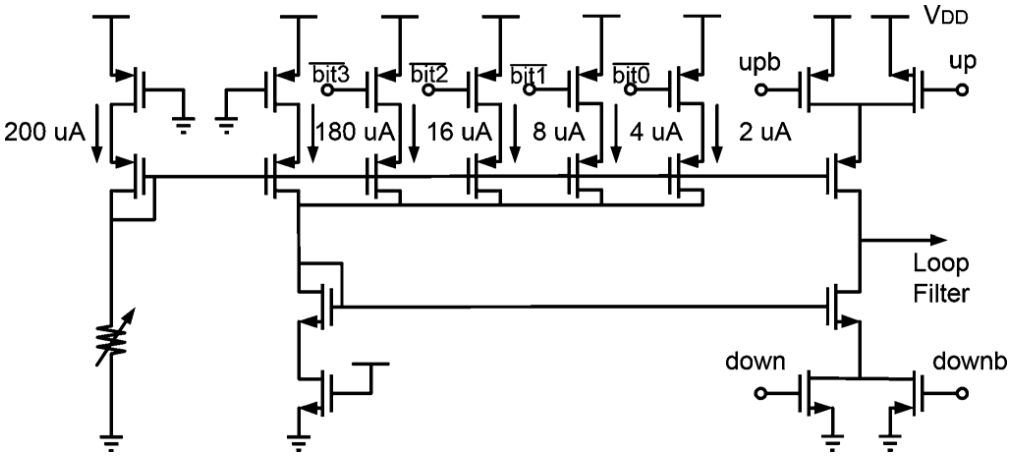

Fig5. *4-bit digitally-controlled charge pump*

Fig. 4 shows the proposed PLL. This PLL is composed of a phase-frequency detector (PFD), a digital-controlled CP, a lock detector (LD), a time-to-digital converter (TDC) [8] with a 4-bit encoder, a self-healing VCO, a programmable divider, and a second-order passive loop filter. The

programmable divider is composed of a 5-bit counter, a 3-bit swallow counter, a modulus control, and a self-healing divide-by-4/5 prescaler. The division ratio is from 4 to 131. When this PLL locks, the LD is enabled to turn on the TDC and an encoder. A 4-bit TDC digitizes this static phase error to reflect the amount of the current mismatching. Then, the digital code of this TDC is used to calibrate the charge pump. The Fig.5 shows the circuit design of the calibrated charge pump

3. IMPLEMENTED RESULT

3.1. Self-Healing Divide-by-4/5 Dual-Modulus Prescaler

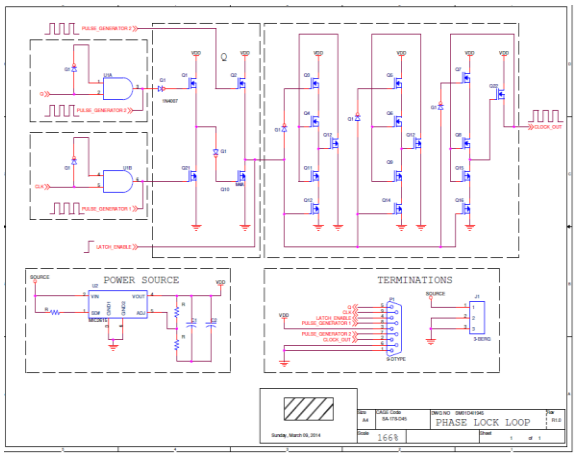

Fig6. *Self-Healing Divide-by-4/5 Dual-Modulus Prescaler Implemented Circuit*

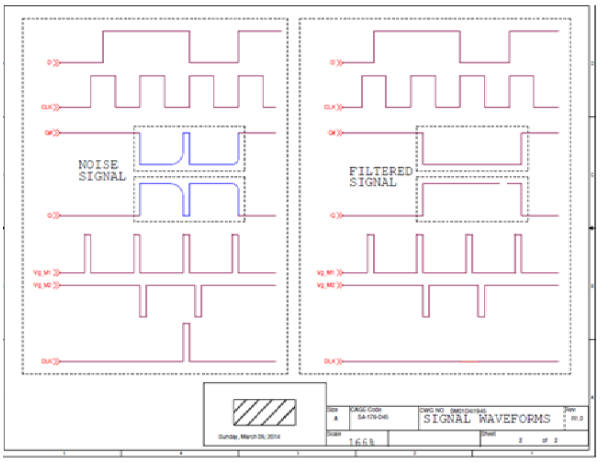

Fig7. *Self-Healing Divide-by-4/5 Dual-Modulus Prescaler Waveform*

3.2. Adaptive PLL

3.2.1. PFD

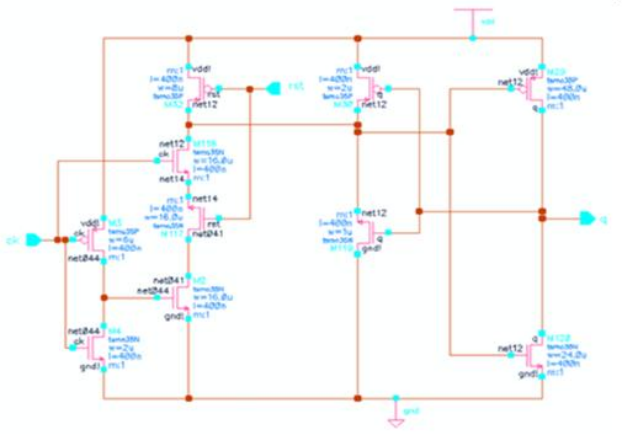

Fig6.3. *Implemented PFD Circuit*

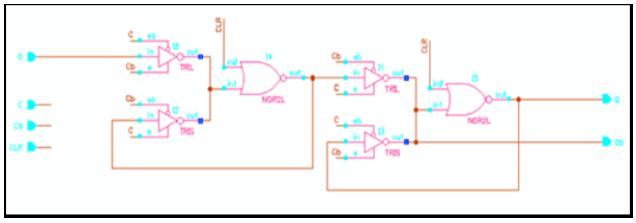

Fig6.4. *Implemented Dff Circuit*

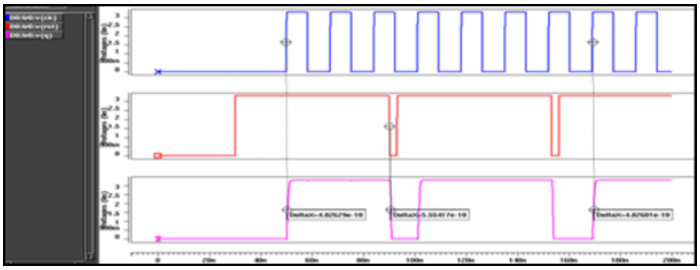

Fig6.5. *Implemented Dff Waveform*

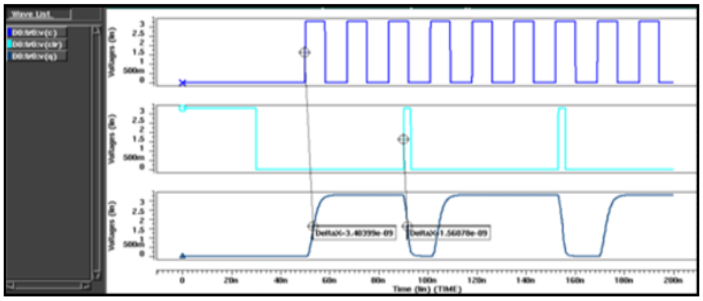

Fig6.6. *Implemented Dff Waveform*

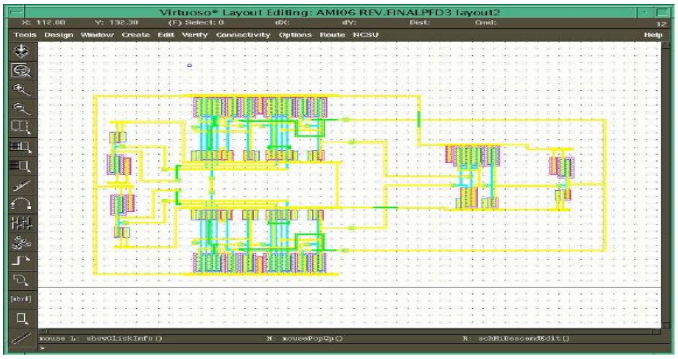

Fig6.7. *Implemented PFD Layout*

3.2.2. Charge Pump

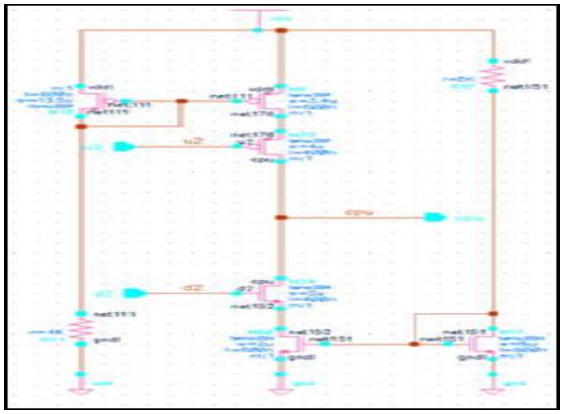

Fig6.8. *Implemented CP Circuit*

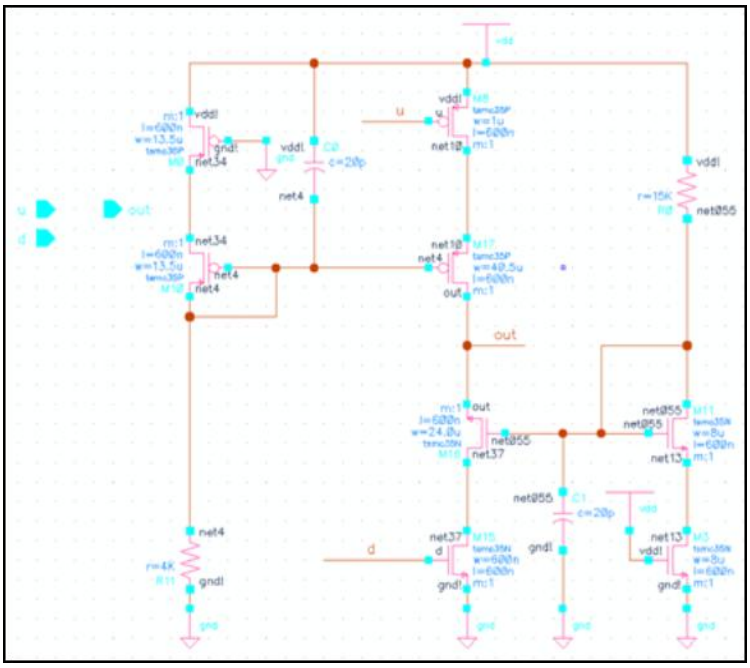

Fig6.9. *Implemented CP with Source Circuit*

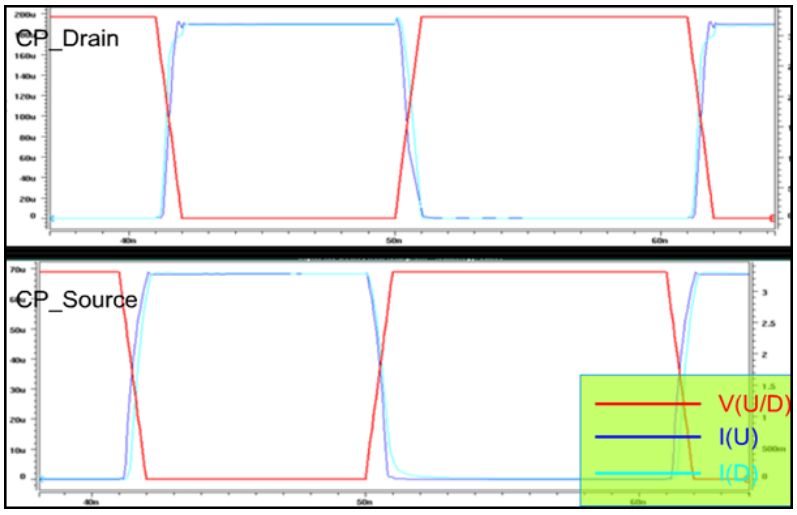

Fig6.10. *Implemented CP Waveform*

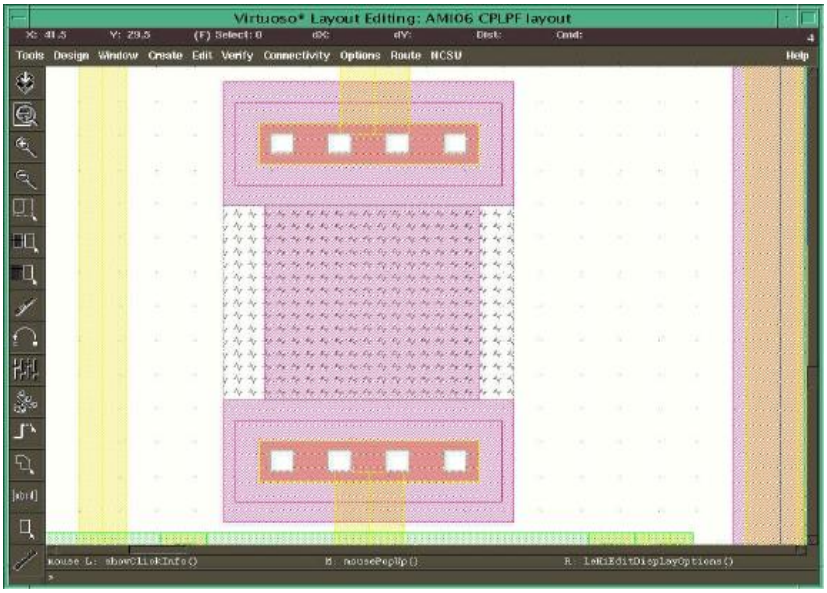

Fig6.11. *Implemented CP Layout*

3.2.3. VCO

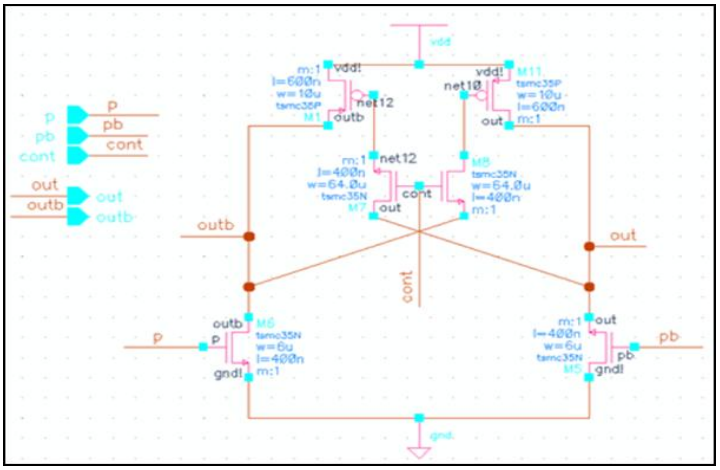

Fig6.12. *Implemented Single Pass VCO Circuit*

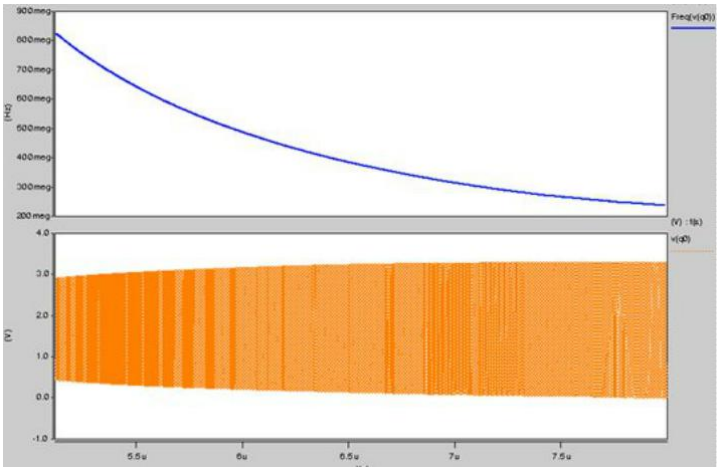

Fig6.13. *Implemented Single Pass VCO Graph and Waveform*

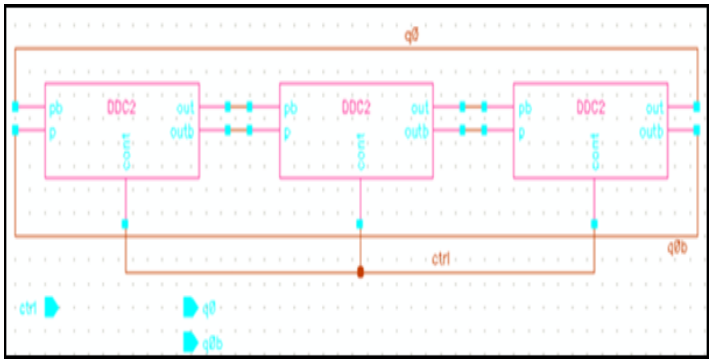

Fig6.14. *Implemented Single Pass VCO Block Circuit*

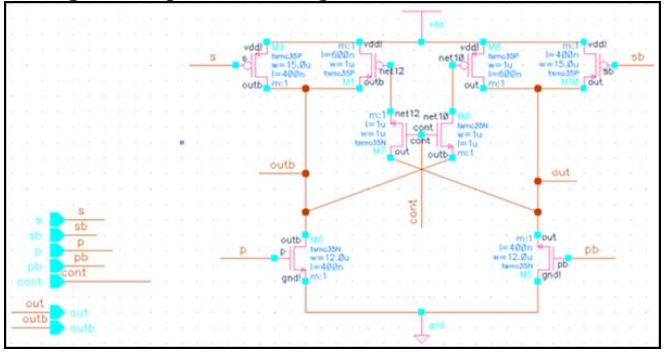

Fig6.15. *Implemented Multiple Pass VCO Circuit*

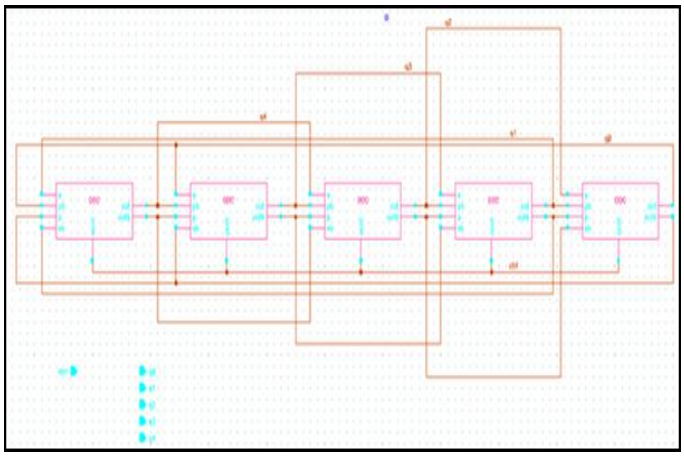

Fig6.16. *Implemented Multiple Pass VCO Block Circuit*

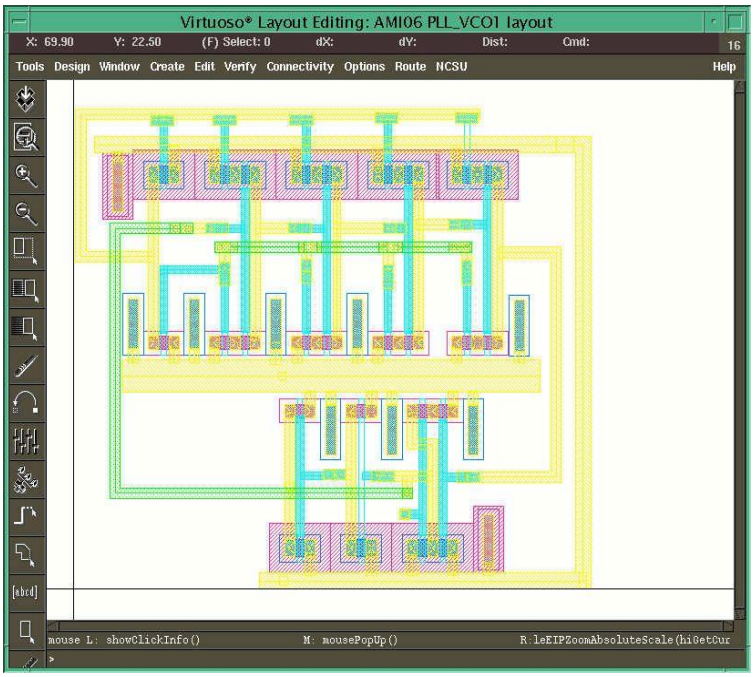

Fig6.17. *Implemented Multiple Pass VCO layout*

3.2.4. Divider Circuit

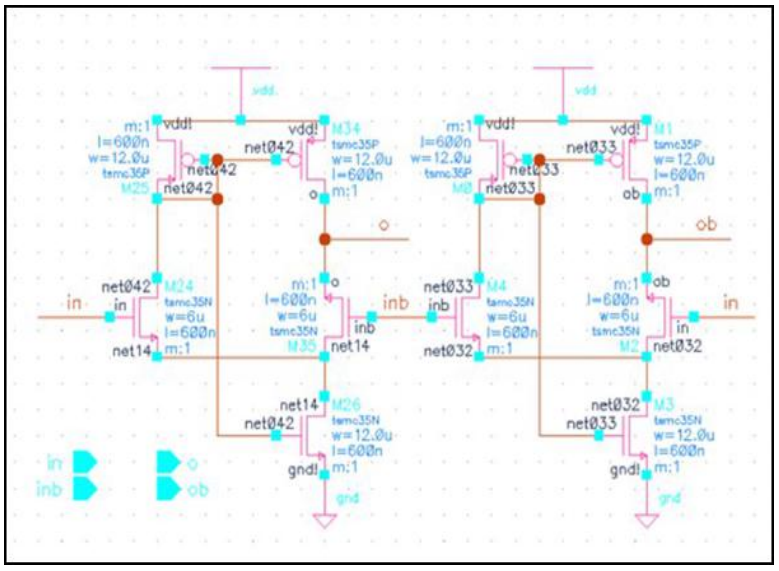

Fig6.18. *Implemented Divider Circuit*

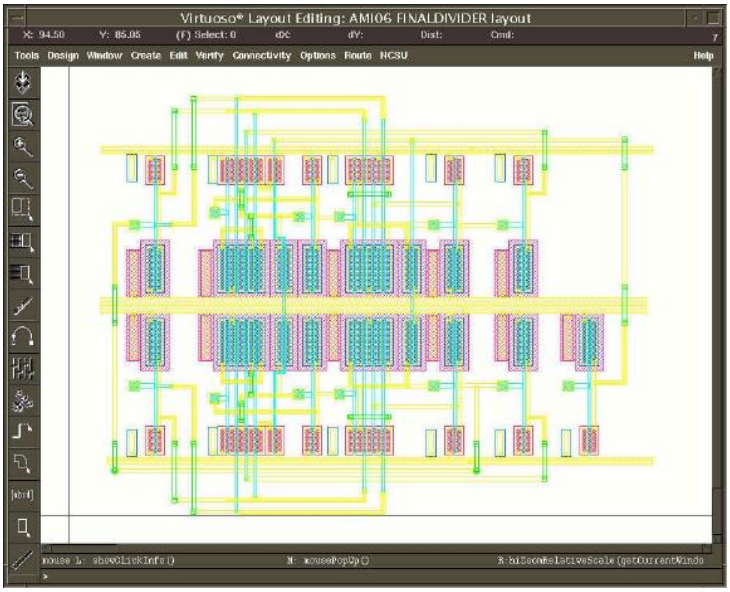

Fig6.19. *Implemented Divider Layout*

3.2.5. Complete PLL

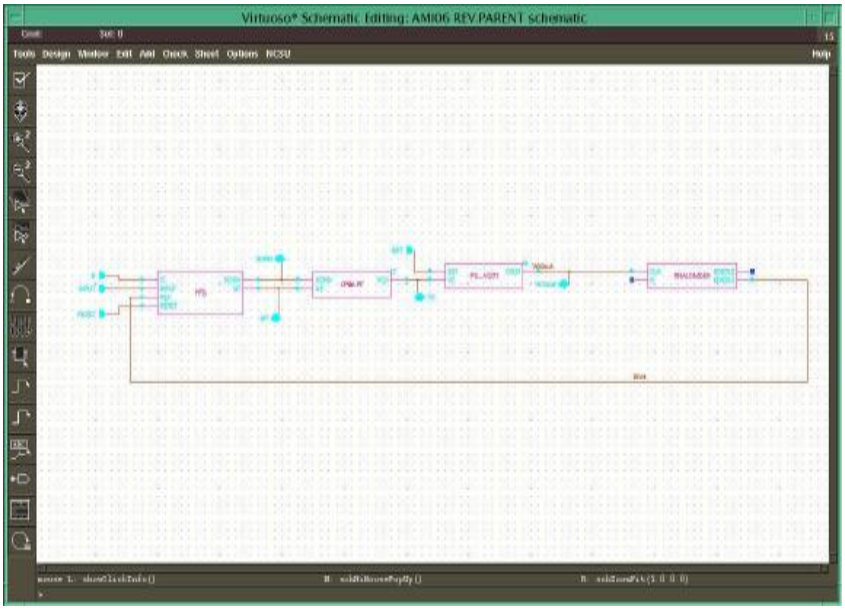

Fig6.20. *Implemented Complete PLL*

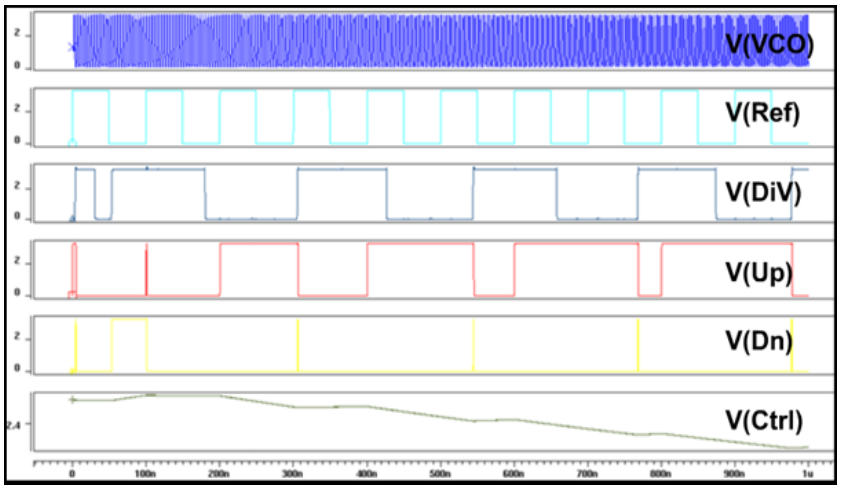

Fig6.21. *PLL Waveform*

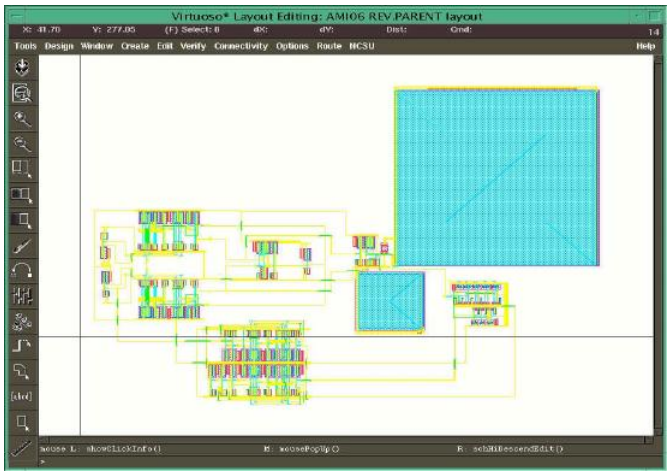

Fig6.22. *Implemented PLL layout*

4. PLL CONNECTED TO SPECTRUM ANALYZER

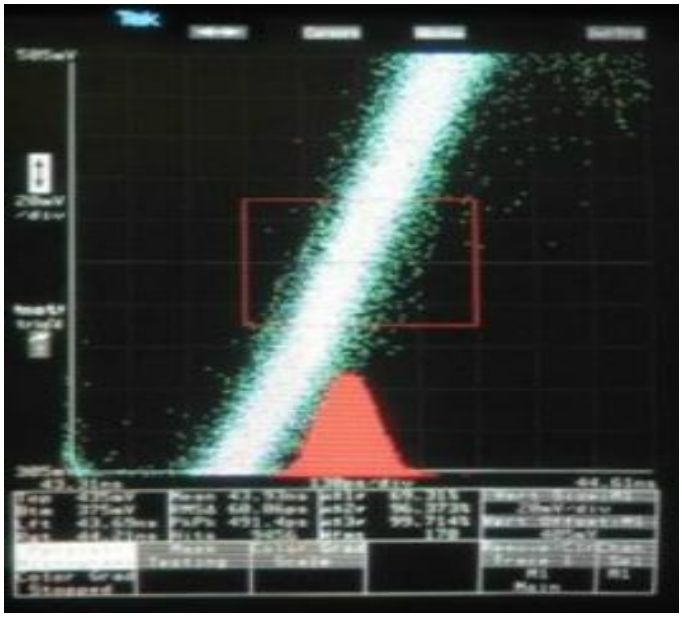

Fig6.23. *Leakage Current Spectrum of the PLL*

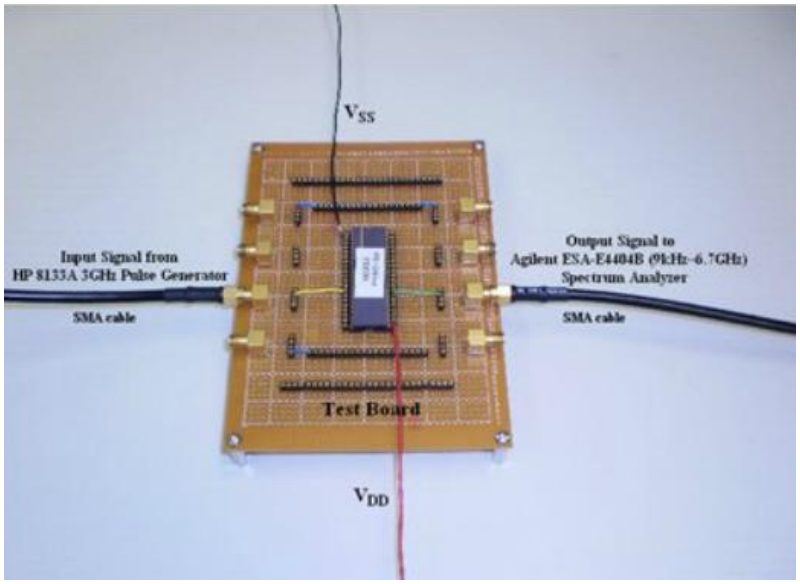

Fig6.24. *Implemented Design Connected to Spectrum Analyzer*

5. CONCLUSION

An adaptive PLL is implemented in a 180-nm CMOS process. To deal with the process variability and leakage current in nanoscale CMOS process, a self-healing prescaler, a self-healing VCO, and a calibrated CP will minimize the leakage current.

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